ALC5651

Ultra-Low Power Two-Channel Audio CODEC with SounzReal™ Digital Sound Effect for Mobile Devices

Datasheet

Rev. 0.9

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC5651 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2012/6/29	Preliminary version
0.2	2012/10/1	Modify typos
0.3	20130308	Modify order information Modify power on/off sequence

Table of Contents

List of Tables

List of Figures

1. General Description

The ALC5651 is a high performance, low power, dual I^2S interface audio CODEC. First I2S interface can support dual mode: normal I2S and I2S with TDM (Time Division Multiplexing) interface. The TDM interface can transmit/receive up to 8 channels data. The transmitted data can from analog input or digital microphone input. Also the received data can to headphone output, line output or PDM output. Asynchronous Sample Rate Converter (ASRC) provides independent and asynchronous connections to different processors, such as an application processor, baseband processor or wireless transceiver(BT).

The Pulse Density Modulation (PDM) output interface can drive external PDM Class-D amplifier. The PDM interface is also build in 8-bits pattern control function for control external PDM amplifier.

The ALC5651 features an ultra low power cap-free headphone amplifier. It consumes only less than 5.5mW power during playback, providing mobile system longer battery life under headphone listening mode.

The integrated DRC(Dynamic Range Controller) and 7-band parametric Equalizer provide further digital sound processing capability of audio playback paths. The DRC in ALC5651 continuously monitors the DAC output level. When the power level is low, it increases the input signal gain to make it sound louder. At the same time, if a peaking signal is detected, it autonomously reduces the applied gain to avoid hard clipping. It ensures the maximum/consistent signal amplitude without producing audio clipping and speaker damage. The 7-band parametric Equalizer contains 7 independent filters with programmable gain, center frequency and bandwidth to tailor the frequency characteristics of embedded speaker system according to user preferences.

For microphone recording, the DRC in ALC5651 can be used as AGC(Auto Gain Controller) to maintain a constant recording volume. Besides, a dynamic wind reduction filter is built in on recording path. The filter can detect the level of wind noise and on/off dynamically to keep the recording quality.

SounzReal^{TM} digital sound effect technology is configurable to provide better listening experience. OminiSound EXP^{TM} expands the sound field of embedded stereo speaker. BassBack EXP^{TM} (low frequency effect) to listeners without subwoofer needed. TruTreble EXP^{TM} adds processed harmonic tones at high frequency, bringing more melody and details for music listening.

ALC5651 only requires two voltage supplies and consume ultra low power, making it ideal for mobile devices.

2. Features

Analog Features:

- Digital-to-Analog Converter with 100dBA SNR
- Analog-to-Digital Converter with 94dBA SNR
- Differential analog microphone inputs with boost pre-amplifiers and low noise microphone bias
  - +20/+24/+30/+35/+40/+44/+50/+52 dB microphone boost gain
  - MIC input to ADC with 50dB boost gain, SNR > 66dBA and THD+N < -65dB
  - Adjustable MICBIAS (0.9*MICVDD or 0.75*MICVDD)
- Stereo line inputs
  - Line input to ADC with 0dB gain, SNR >= 94dBA, THD+N <= -83dB
- Stereo line outputs
  - DAC to line output with 0dB gain, SNR >= 100dBA, THD+N <= -86dB
- Stereo Cap-Free headphone amplifier with ultra low power consumption for playback
  - 20mW/CH (AVDD=CPVDD=1.8V, THD+N <= -80dB, 16Ohm Load)
  - Playback power consumption <= 5.5mW (AVDD=VBVDD=CPVDD=1.8V, 16Ohm, With I2S Clock, Playback Silence)
  - Playback power consumption <= 13mW (AVDD=VBVDD=CPVDD=1.8V, 16Ohm, With I2S Clock, Playback 1mW/CH)
- Audio jack insert/combo jack detection
- Inside PLL can receiver wide range clock input

Digital Features:

- One 24bit/8kHz ~ 192kHz I^2S/PCM/TDM interface for stereo DAC and stereo ADC
- One 24bit/8kHz ~ 192kHz I^2S/PCM interface for stereo DAC and stereo ADC
- I^2C control interface
- One digital microphone interface support
- Asynchronous sample rate converter (ASRC) for each interface
- 7-bands flexible equalizer (EQ) for DAC path or ADC path
- Enhanced DRC(Dynamic Range Control)/AGC(Auto Gain Control) function for DAC path or ADC path
- One wind noise reduction filter
- Zero detection and soft volume for pop noise suppression
- SounzReal™ audio sound processing
  - OminiSound EXP™
  - TruTreble EXP™
  - BassBack EXP™

3. System Application

- Smart Phones
- Tablet

4. Function Block and Mixer Path

4.1. Function Block

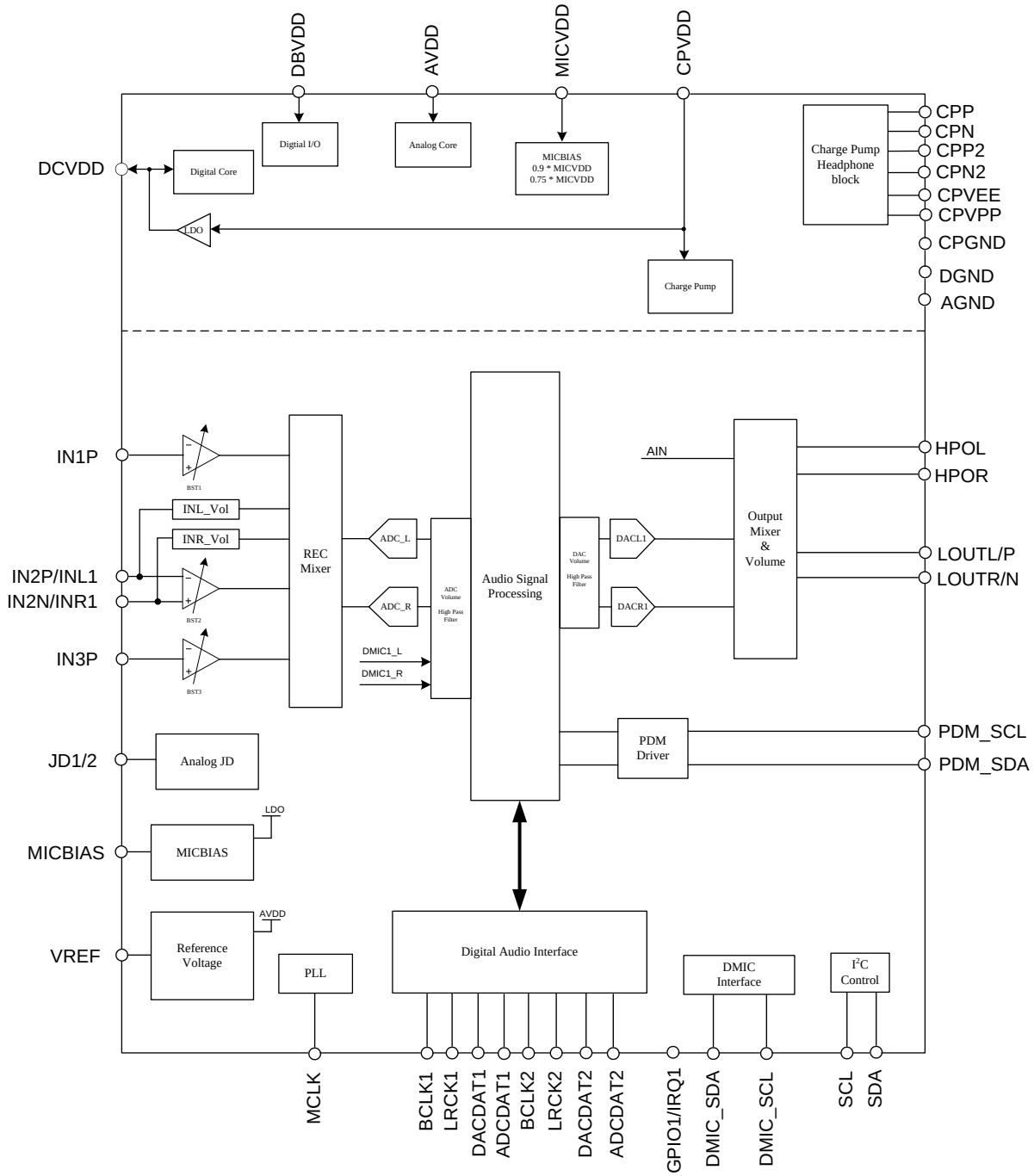


Figure 1. Block Diagram

4.2. Audio Mixer Path

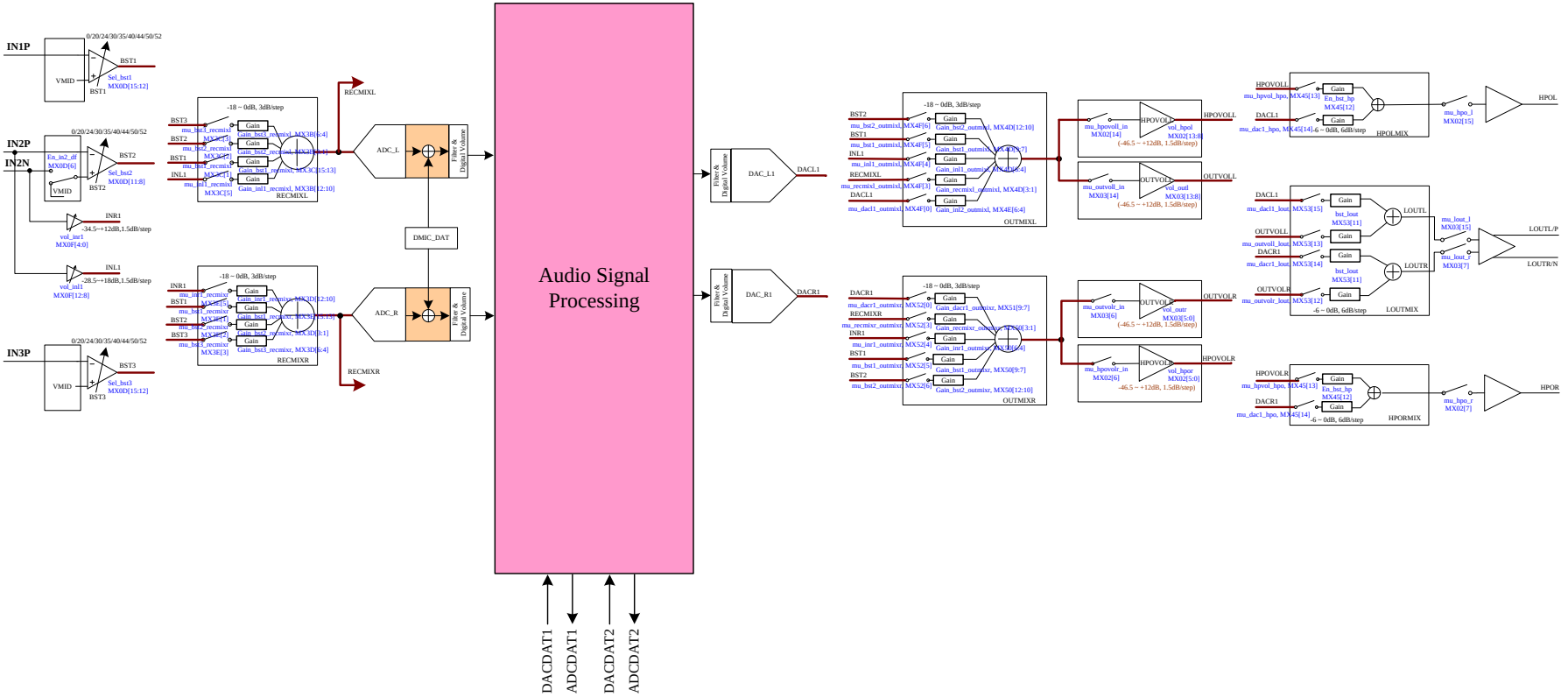


Figure 2. Audio Mixer Path

4.3. Digital Mixer Path

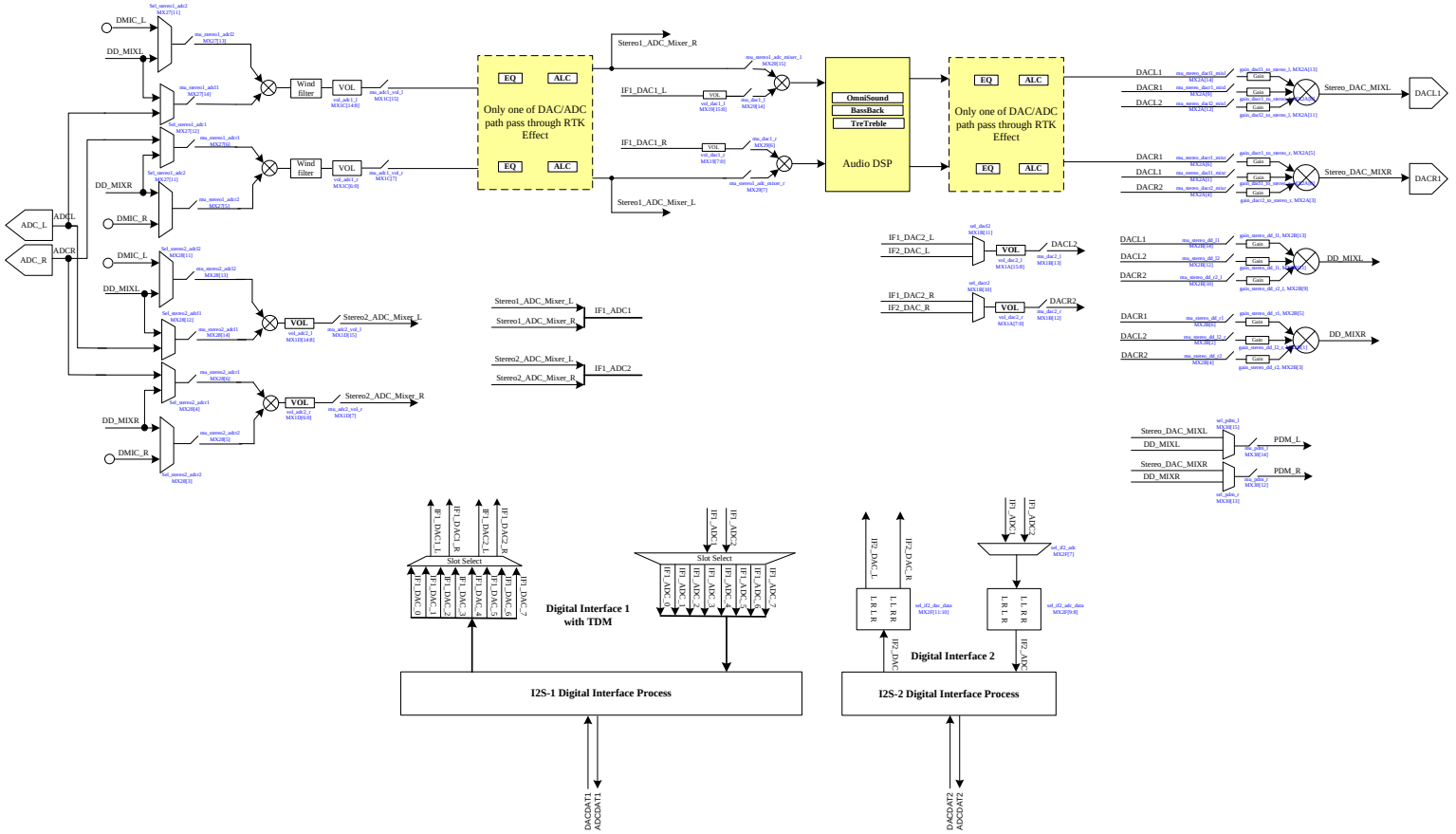


Figure 3. Digital Mixer Path

5. Pin Assignments

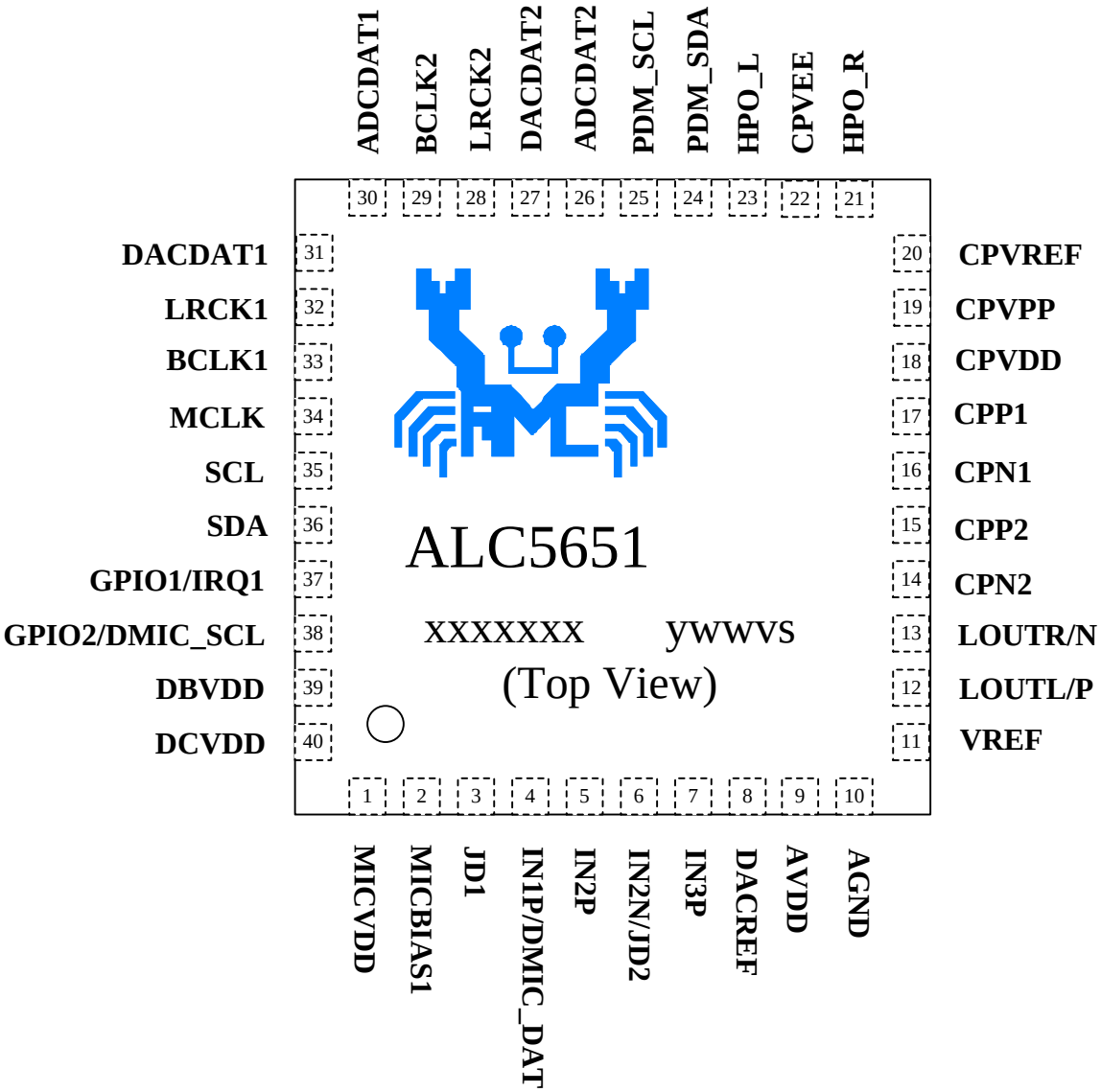


Figure 4. Pin Assignments

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
DACDAT1	I	31	First I2S interface serial data input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
ADCDAT1	O	30	First I2S interface serial data output	V_{OL}=0.1*DBVDD, V_{OH}=0.9*DBVDD
BCLK1	I/O	33	First I2S interface serial bit clock	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
LRCK1	I/O	32	First I2S interface synchronous signal	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
DACDAT2	I	27	Second I2S interface serial data input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
ADCDAT2	O	26	Second I2S interface serial data output	V_{OL}=0.1*DBVDD, V_{OH}=0.9*DBVDD
BCLK2	I/O	29	Second I2S interface serial bit clock	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
LRCK2	I/O	28	Second I2S interface synchronous signal	Master: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Slave: Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
SDA	I/O	36	I2C interface serial data	Open drain structure
SCL	I	35	I2C interface clock input	Schmitt trigger
MCLK	I	34	I2S interface master clock input	Schmitt trigger (V_{IL}=0.35*DBVDD, V_{IH}=0.65*DBVDD)
GPIO1/IRQ	I/O	37	General purpose input and output Interrupt output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger
GPIO2/ DMIC_SCL	I/O	38	General purpose input and output Digital microphone clock output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD Input: Schmitt trigger
PDM_SCL	O	25	PDM clock output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD
PDM_SDA	O	24	PDM data output	Output: V_{OL} =0.1*DBVDD, V_{OH} =0.9*DBVDD
				Total: 15 Pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LOUTR/N	O	13	Line output type Right channel single-end output Negative channel differential output	Analog output
LOUTL/P	O	12	Line output type Left channel single-end output Positive channel differential output	Analog output
IN2P	I	5	Positive differential input for microphone 2 Left channel line input	Analog input
IN2N/JD2	I	6	Negative differential input for microphone 2 Right channel line input Second jack detection pin	Analog input JD threshold: V_{IL} = 0.5V, V_{IH} = 1.2V
IN1P/DMIC_DAT	I	4	Single-end input for microphone 1 Digital microphone data input	Analog input Digital input
JD1	I	3	First jack detection pin	Multi-level jack detection pin JD threshold: V_{t1} = 1.485V V_{t2} = 1.925V V_{t3} = 2.7V
HPO_R	O	21	Headphone amplifier output Right channel	Analog output
HPO_L	O	23	Headphone amplifier output Left channel	Analog output
IN3P	I	7	Single-end input for microphone 3	Analog input
				Total: 9 Pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
MICBIAS1	O	2	Bias voltage output for microphone	Programmable analog DC output
VREF	O	11	Internal reference voltage	4.7uF capacitor to analog ground
CPVREF	-	20	Headphone reference ground	Headphone ground
CPN1	-	16	First charge pump bucket capacitor	2.2uf capacitor to CPP1
CPP1	-	17	First charge pump bucket capacitor	2.2uf capacitor to CPN1
CPN2	-	14	Second charge pump bucket capacitor	2.2uf capacitor to CPP2

Name	Type	Pin	Description	Characteristic Definition
CPP2	-	15	Second charge pump bucket capacitor	2.2uf capacitor to CPN2
				Total: 7 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
MICVDD	P	1	Analog power for MICBIAS	3.0V ~ 3.3V (Default 3.3V is recommended)
AVDD	P	9	Analog power	1.71V ~ 1.9V (Default 1.8V is recommended)
DACREF	P	8	Analog power	1.71V ~ 1.9V (Default 1.8V is recommended)
AGND	P	10	Analog ground	
CPVDD	P	18	Analog power for headphone charge pump	1.71V ~ 1.9V (Default 1.8V is recommended)
CPVEE	P	22	Charge pump negative voltage output	2.2uf capacitor to analog ground
CPVPP	P	19	Charge pump positive voltage output	2.2uf capacitor to analog ground
DCVDD	P	40	Digital power for digital core. Kept open if LDO1_EN is pulled high, or connected to external 1.2V power.	1.1V~1.3V (Default open is recommended. Pull high LDO1_EN to DBVDD to general 1.2V DCVDD by internal LDO. It can be connected to external 1.2V if LDO1_EN is pulled low.)
DBVDD	P	39	Digital power for digital I/O buffer	1.71V~3.3V (Default 1.8V is recommended)
CPGND/ DGND	P	41*	Charge pump ground Digital ground	Exposed-Pad
				Total: 9 Pins

7. Function Description

7.1. Power

There are different power types in ALC5651. DBVDD is for digital I/O power, DCVDD is for digital core power, AVDD and DACREF are for analog power, CPVDD is for charge pump power, MICVDD is for MICBIAS power.

The power supplier limit condition are DBVDD ≧ DCVDD and MICVDD > AVDD = DACREF = CPVDD, AVDD ≧ DCVDD, and for the best performance, our design setting is show on below.

Table 5. Power Supply for Best Performance

Power	DBVDD	DCVDD	AVDD	DACREF	CPVDD	MICVDD
Setting	1.8V	1.2V	1.8V	1.8V	1.8V	3.3V

*1.2V DCVDD was generated by internal LDO.

To prevent all power down leakage, needs keep all power supply on.

Table 6. Power Supply Condition for Power Down Leakage

Power	DBVDD	AVDD	DACREF	CPVDD	MICVDD
Setting	Supplied	Supplied	Supplied	Supplied	Supplied

7.2. Power Supply On/Off Sequence

To prevent pop noise and make sure function work normally, following power on and off sequence are recommended.

Power On Sequence: (Sequentially turn on power pins)

1. DBVDD/AVDD/DACREF/CPVDD=1.8V power supply on.
2. DBVDD power supply on (If DBVDD is higher than 1.8V)
3. MICVDD power supply on.
4. Software starts to initialize ALC5651.

Power Off Sequence: (Sequentially turn off power pins)

1. Power down all Codec function (Write 0x0000'h to register MX-00'h).
2. MICVDD power supply off.
3. DBVDD power supply off (If DBVDD is higher than 1.8V)
4. DBVDD/AVDD/DACREF/CPVDD=1.8V power supply off

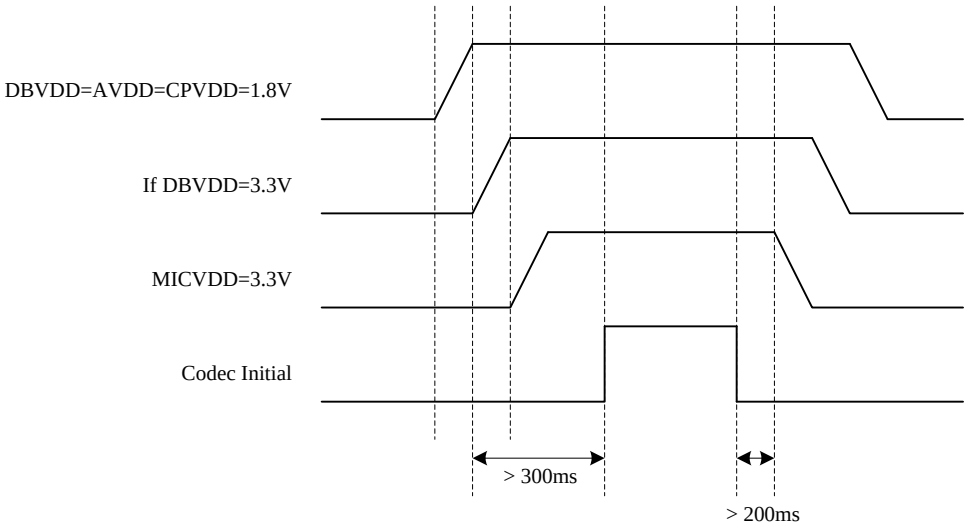


Figure 5. Power On/Off Sequence

7.3. Reset

There are 2 types of reset operation: power on reset (POR) and register reset.

Table 7. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Reset all hardware logic and all registers to default values.
Register Reset	Write MX-00h	Reset all registers to default values except some specify control registers and logic.

7.3.1. Power-On Reset (POR)

When powered on, DCVDD passes through the V_{POR} band of the ALC5651 (V_{POR_ON} ~V_{POR_OFF}). A power on reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 8. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	-	0.8	-	V
V_{POR_OFF}	-	0.52	-	V

Note:
1.V_{POR_OFF} must be below V_{POR_ON}
2. $T^oC = 25^oC$
3. When DCVDD is supplied 1.2V

7.3.2. Software Reset

When MX-00h is wrote, all registers become to default value.

7.4. Clocking

The system clock of ALC5651 can be selected from MCLK or PLL. MCLK is always provided externally while the reference clock of PLL can be selected from MCLK, BCLK1/2. The driver should arrange the clock of each block and setup each divider.

The Clk_sys_i2s1=256*Fs provides clocks into stereo1 DAC/ADC filter that can be selected from MCLK or PLL. Refer to Figure 5. Audio SYSCLK
The Clk_sys_i2s2=256*Fs provides clocks into stereo2 DAC/ADC filter that can be selected from MCLK, PLL, refer to Figure 5. Audio SYSCLK

When enable ASRC (Asynchronous Sample Rate Converter) function, the clock sources from MCLK and BCLK1 (or BCLK2) are allowed to be asynchronous. The Realtek ASRC technology can ensure data accuracy and keep audio performance under clock source asynchronous.

When ALC5651 at master mode, the clock source from MCLK will be divided and be sent to external device. The ratio of BCLK and LRCK can set by register – MX73/77.

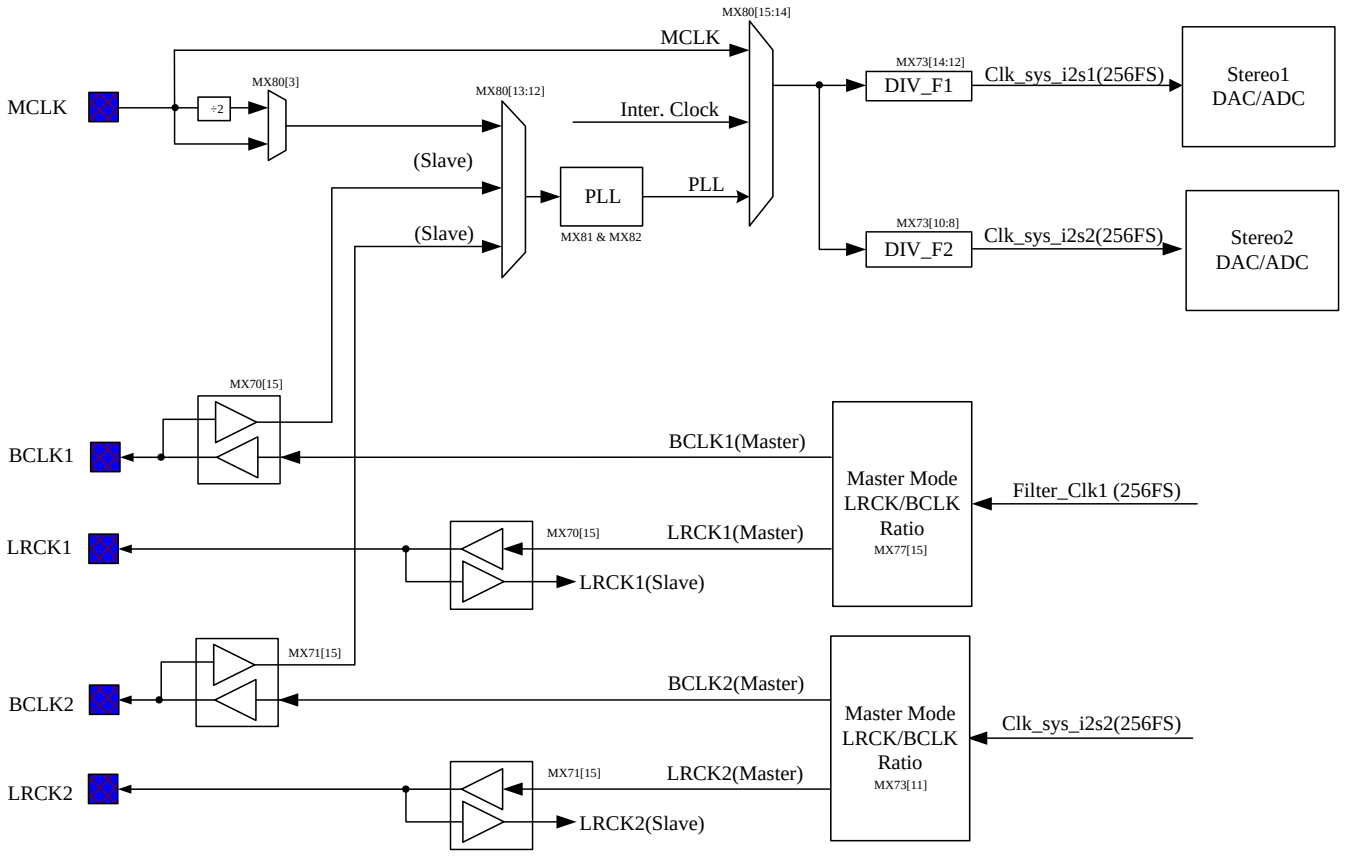


Figure 6. Audio Clock Tree

7.4.1. Phase-Locked Loop

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz to 40MHz. The source of the PLL can be set to MCLK, BCLK1 or BCLK2 by setting register.

The S/W driver can set up the PLL to output a frequency to match the requirement of system clock.

The PLL transmit formula as below:

F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) {Typical K=2}

Table 9. Clock Setting Table for 48K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6
24	39	8	98.4	2	24.6

Table 10. Clock Setting Table for 44.1K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632
24	62	15	90.352	2	22.588

7.4.2. I²C and I²S/PCM/TDM Interface

The ALC5651 supports I²C for the digital control interface, and has one I²S/PCM/TDM for first digital data interface and one I²S/PCM for second digital data onterface. These two I²S/PCM/TDM audio digital interfaces are used to send data to 4 DACs or to receive data from a stereo ADC. The two I²S/PCM/TDM audio digital interfaces are also can be configured to Master mode or Slave mode.

Master Mode

Under master mode, BCLK and LRCK are configured as output. If I2S SYSCLK is selected from MCLK source, sel_sysclk1 (MX-80[15:14]) should set as 00'b. If selected from PLL output, sel_sysclk1 should set as 01'b. PLL's source is suggested to provide frequency from 2.048MHz to 40MHz. The driver should set each divider (MX-73 and MX-89) to arrange the clock distribution. Refer to Figure5. Audio Clock Tree, for details.

Table 11. The relative of SYSCLK/BCLK/LRCK

Register Settings	MCLK	BCLK	LRCK
MX-73[15]=0'b	256*FS=12.288MHz	32*FS=1.536MHz	FS=48KHz
MX-73[15]=1'b	256*FS=12.288MHz	64*FS=3.072MHz	FS=48KHz
MX-73[15]=0'b	256*FS=11.2896MHz	32*FS=1.4112MHz	FS=44.1KHz
MX-73[15]=1'b	256*FS=11.2896MHz	64*FS=2.8224MHz	FS=44.1KHz

Example for master mode:
Target format:
Sample Rate: 48 KHz
Channel Length: 32 bits
LRCK=48KHz
BCLK=3.071MHz (64 * 48KHz)

MCLK clock request:
MCLK=12.288MHz (256 * 48 KHz)

Register settings:
Set MX-FA[0] to "1" // For MCLK input clock getting control
Set MX-61[15] to "1" // Enable I2S-1
Set MX-70[15] to "0" // Enable Master mode

Slave Mode

Under slave mode BCLK and LRCK are configured as input. The SYSCLK can be input from MCLK and BCLK can be synchronous or asynchronous to MCLK. If the SYSCLK is selected from BCLK, the internal PLL should generate 256*FS by BCLK. And the driver should set each divider to arrange the clock distribution. Refer to Figure5. Audio Clock Tree, for details.

If an asynchronous MCLK input for BCLK and LRCK, you can turn ASRC function for this situation. As Figure 6 shown, the MCLK is from external oscillator that clock is no relation (or asynchronous) with SOC and BT or 3G BaseBand. For the connection, SOC and BT can connect directly to Codec and let Codec as slave mode and SOC/BT as master mode.

For the clock requirement of MCLK must large than 512*FS as SYSCLK that FS is sample rate. If the MCLK is smaller than 512*FS, that can use internal PLL to generate higher than 512*FS clock.

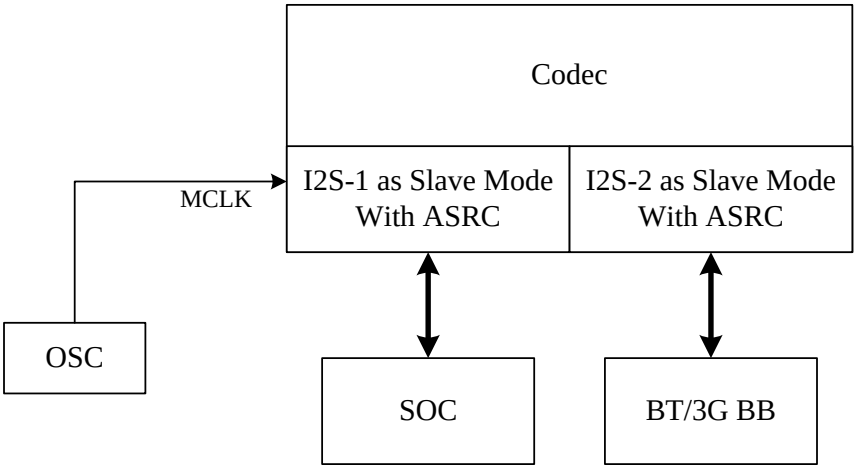


Figure 7. System Connection for ASRC Function

The following table shows the related path application for ASRC register settings.

Table 12. Register Settings for ASRC Function on Slave Mode

Condition: **Codec as Slave Mode** **MCLK = 12MHz** **Frame Rate = 64*FS** **Target Sample Rate (FS) = 48KHz**		
Item	**Register Settings**	**Note**
PLL Settings	TBD	PLL settings to generate 512*FS (24.576MHz) for SYSCLK
I2S-1 to DAC1	TBD	For DAC1 playback ASRC settings
I2S-1 to PDM Output	TBD	For PDM output playback ASRC settings
AMIC to Stereo1 ADC Filter to I2S-1	TBD	For AMIC to Stereo1 ADC Filter record ASRC settings
AMIC to Stereo2 ADC Filter to I2S-2	TBD	For AMIC to Stereo2 ADC Filter record ASRC settings
DMIC to Stereo1 ADC Filter to I2S-1	TBD	For DMIC to Stereo1 ADC Filter record ASRC settings

For TDM application, the TDM interface can transmit multi-channel data in one serial interface. ALC5651 can receive and transmit up to 8 channels data. Owing to can receive and transmit multi-channel data, so it can connect multi-codec on one interface, as Figure 7. ALC5651 #1 and #2 share one TDM interface.

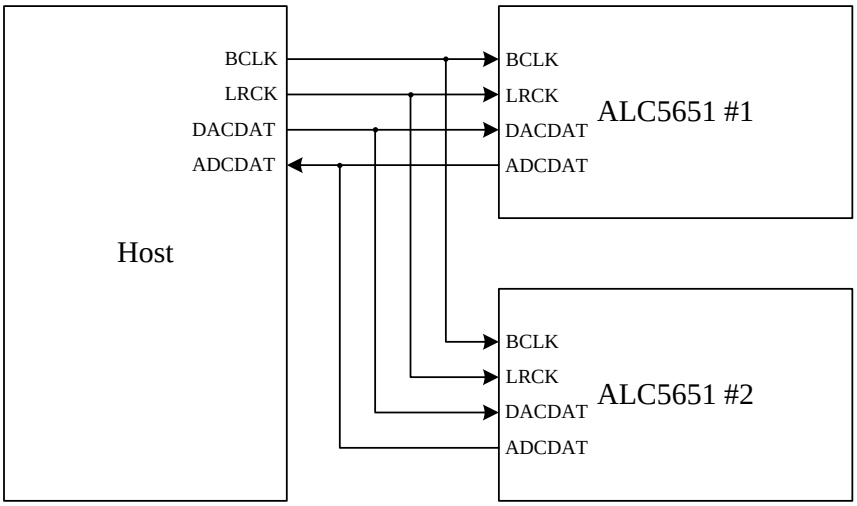


Figure 8. TDM Interface Application - 1

The following figure shows TDM format when connect two ALC5651 Codec. For data receiving by DACDAT pin, ALC5651 #1 only receives channel-0/1 and channel-2/3 received by ALC5651 #2. For data transmitting by ADCDAT pin, ALC5651 #1 will drive data on channel-0/1 and channel-2/3 will float for ALC5651 #2. ALC5651 #2 will drive data on channel-2/3.

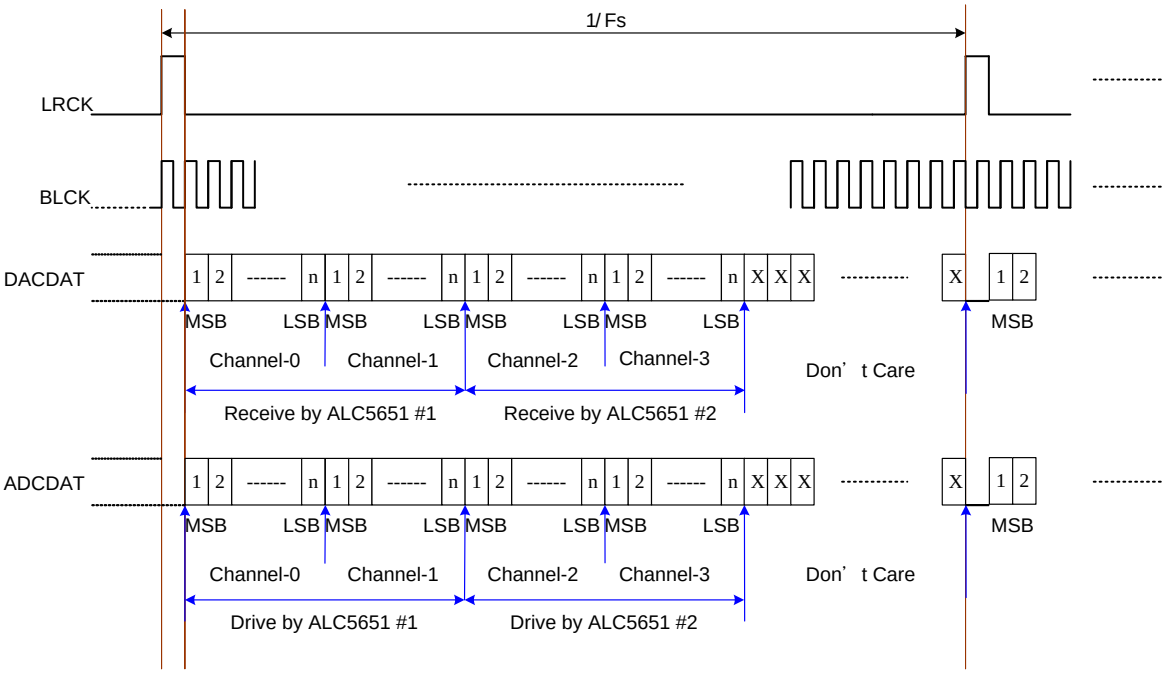


Figure 9. TDM Interface Application - 2

7.5. Digital Data Interface

7.5.1. Two I²S/PCM Interface

The two I2S/PCM interface can be configured as master mode or slave mode. Four audio data formats are supported:

- PCM mode
- Left justified mode
- I²S mode
- TDM mode

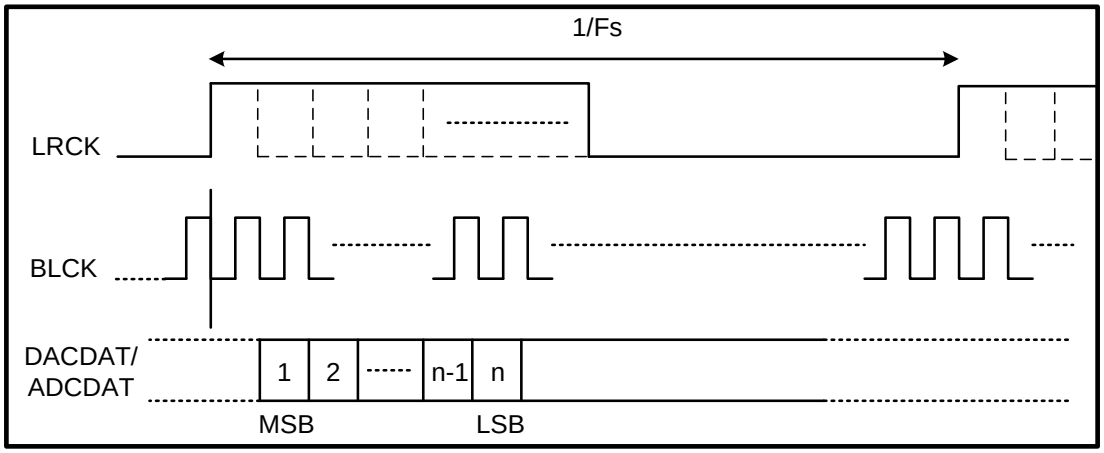


Figure 10. PCM MONO Data Mode A Format (BCLK POLARITY=0)

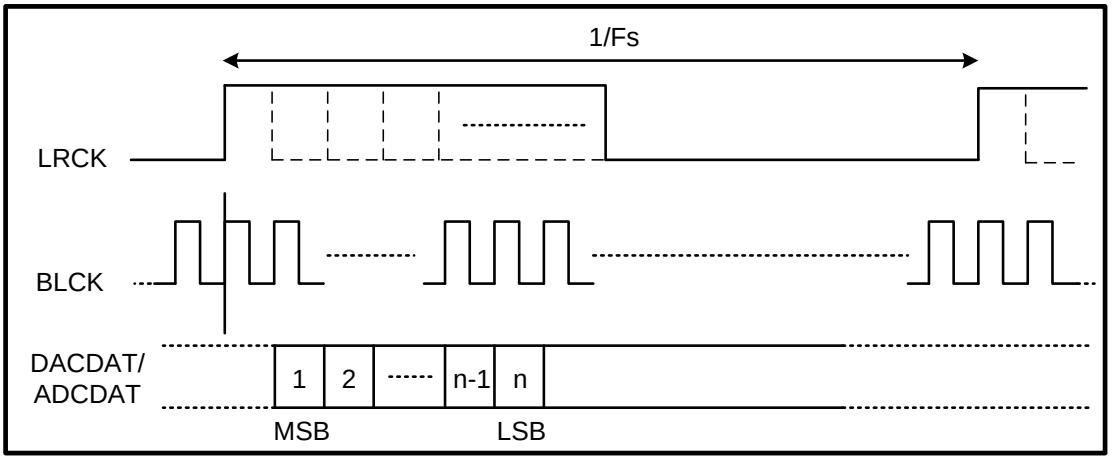


Figure 11. PCM MONO Data Mode A Format (BCLK POLARITY=1)

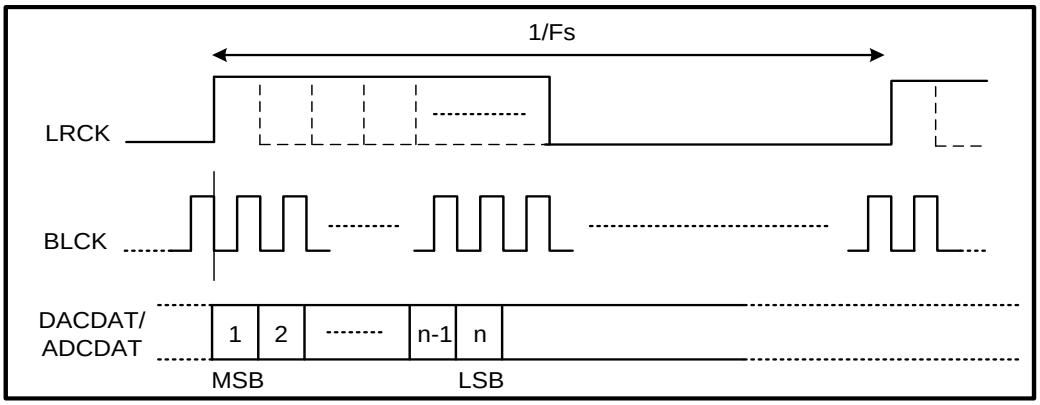


Figure 12. PCM MONO Data Mode B Format (BCLK POLARITY=0)

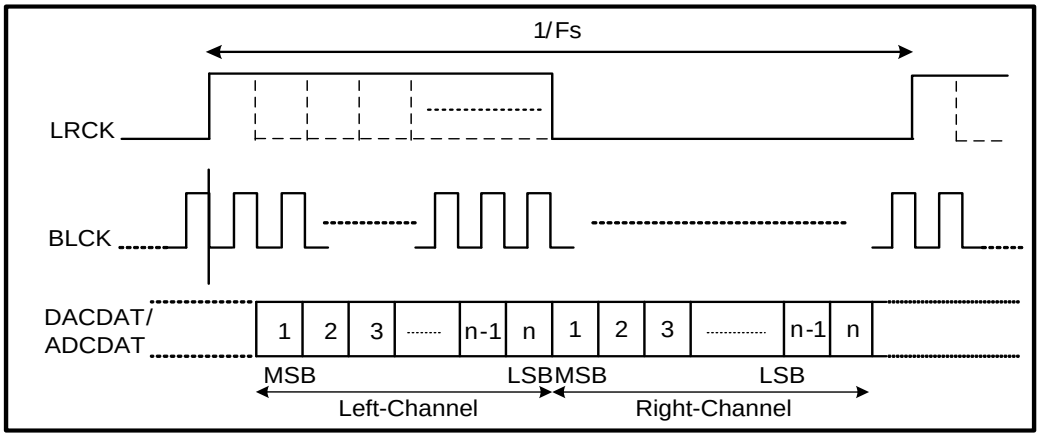


Figure 13. PCM Stereo Data Mode A Format (BCLK POLARITY=0)

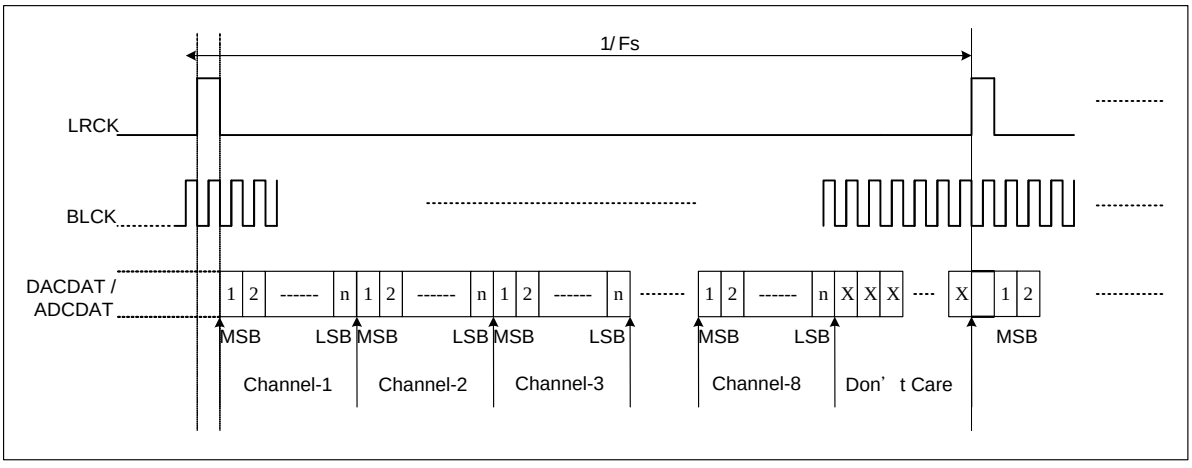


Figure 14. PCM TDM Data Mode A Format (BCLK POLARITY=0)

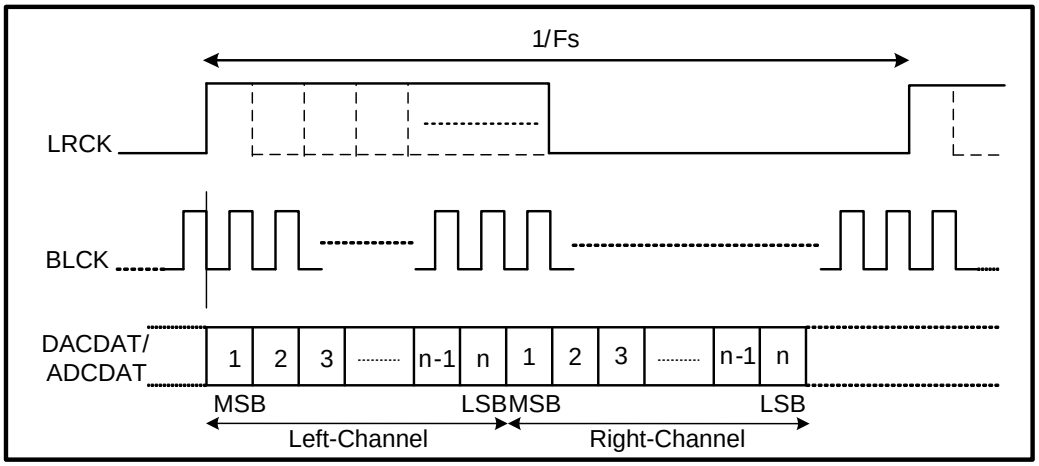


Figure 15. PCM Stereo Data Mode B Format (BCLK POLARITY=0)

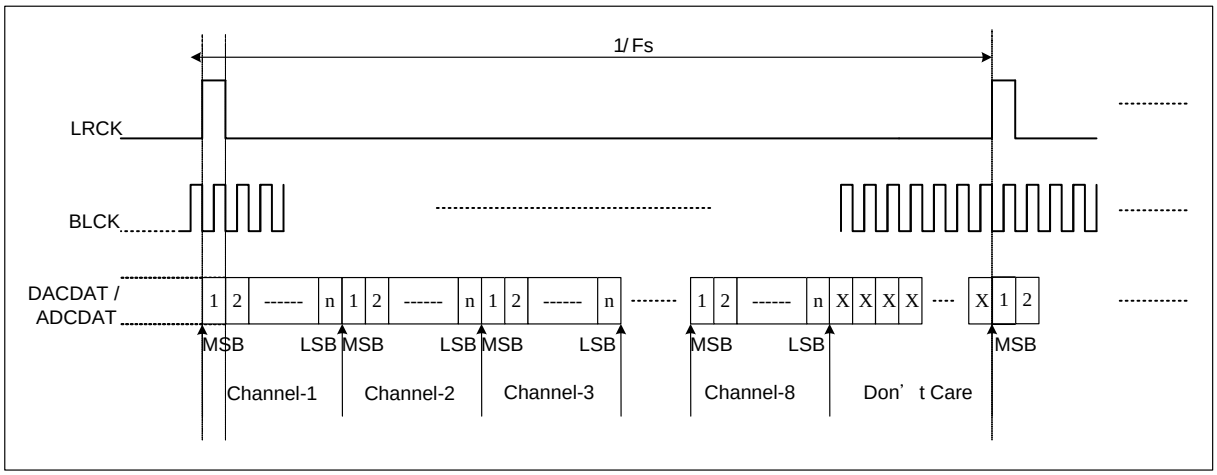


Figure 16. PCM TDM Data Mode B Format (BCLK POLARITY=0)

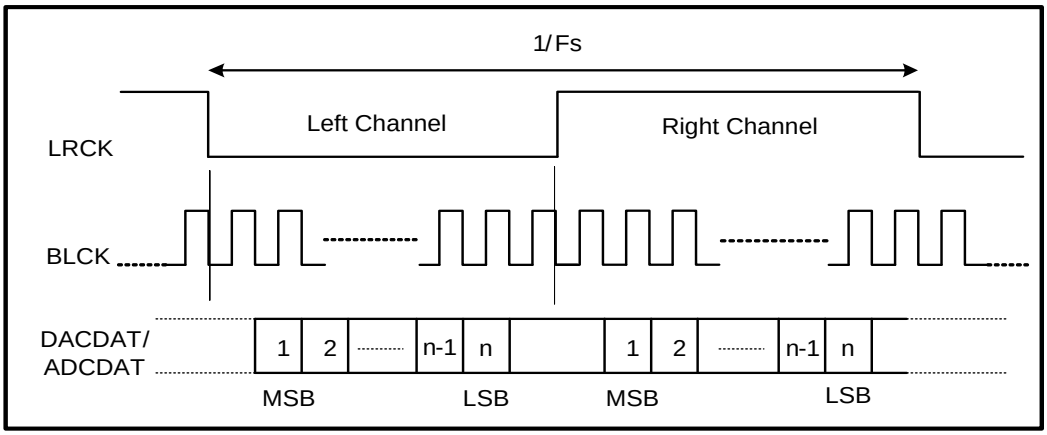


Figure 17. I²S Data Format (BCLK POLARITY=0)

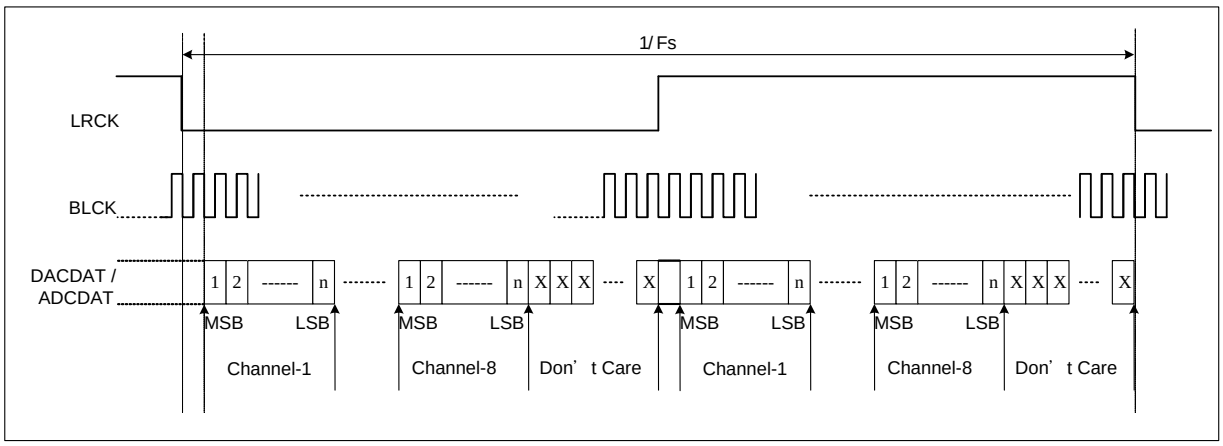


Figure 18. I²S TDM Data Format (BCLK POLARITY=0)

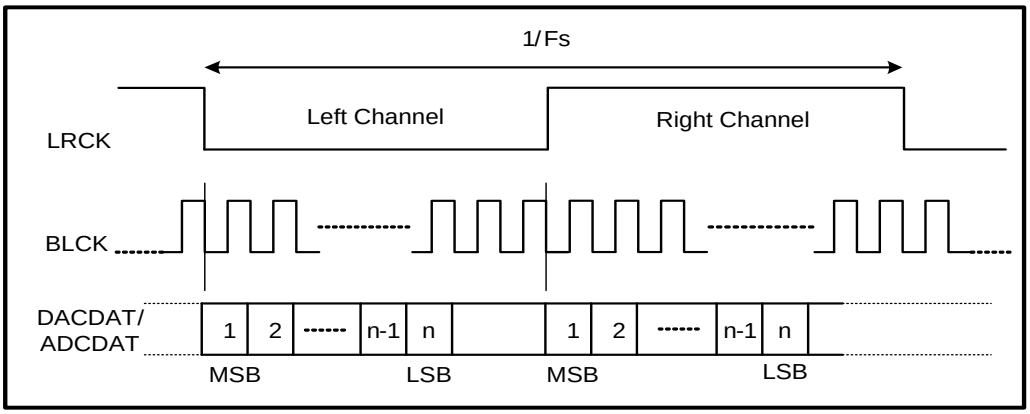


Figure 19. Left-Justified Data Format (BCLK POLARITY=0)

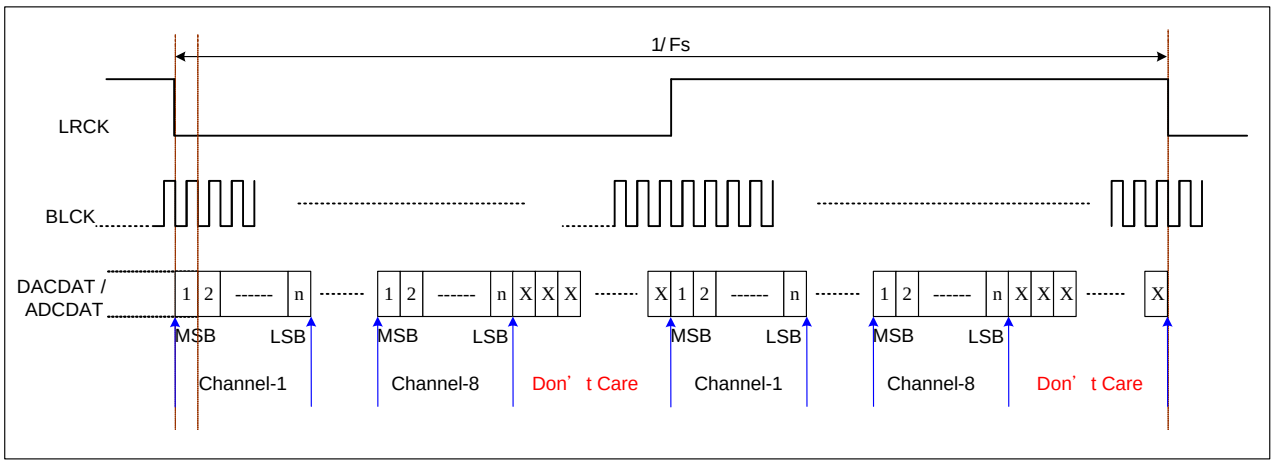


Figure 20. Left-Justified TDM Data Format (BCLK POLARITY=0)

7.6. Audio Data Path

The ALC5651 provides 2-channel analog DACs for playback and 2-channel analog ADCs for recording.

7.6.1. 2 Analog ADCs with 4-Channel Record Path

There are two analog ADCs and with up to 4-channel recording path. You can use two analog microphones pass to analog ADCs and two digital microphones to reach 4-channel recording. Or use two digital microphone interfaces to reach 4-channel recording. These 4-channel data can pass to 2-I2S interface or TDM interface.

The full scale input of analog ADC is around 0.7Vrms. In order to save power, the left and right analog ADC can be powered down separately by setting pow_adc_l (MX-61[2]) and pow_adc_r (MX-61[1]). And the volume control of the stereo ADC is also separately controlled by ad_gain_l (MX-1C[14:8]) and ad_gain_r (MX-1C[6:0]).

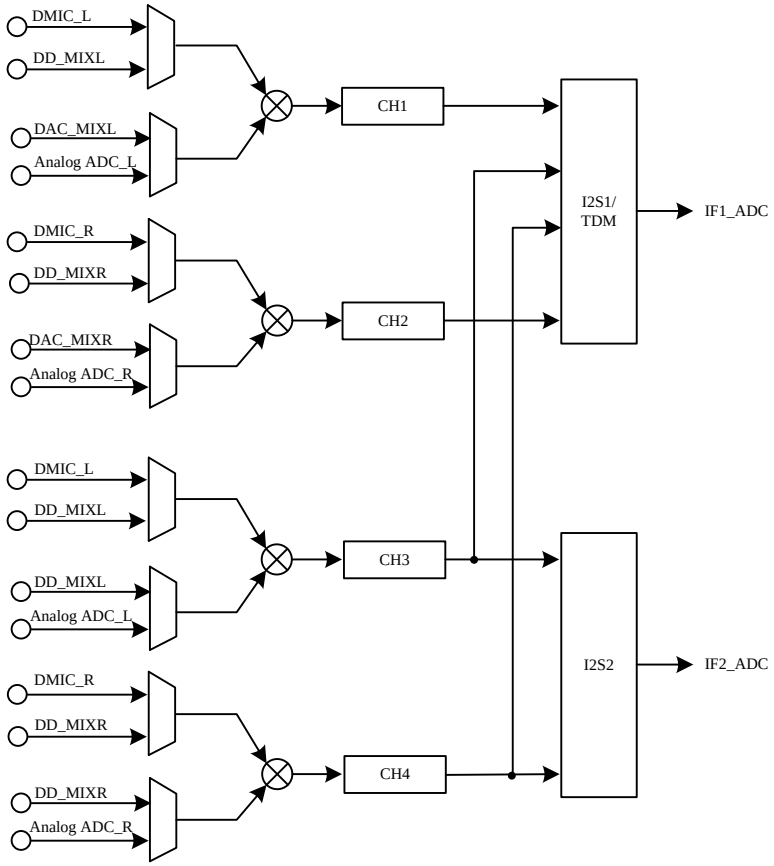


Figure 21. 4-Channel Recording Path

7.6.2. 2 DACs with 4-Channel Playback Path

There are two analog DACs and with up to 4-channel playback path. Two I2S interfaces provide four channels data to analog DACs or PDM output. Or one TDM interface provide four channels data to analog DACs or PDM output. The analog DACs can output audio signal to headphone output or line output.

The full scale output of analog DAC is around 1Vrms at line output port. In order to save power, the two analog DACs can be powered down separately by setting pow_dac_l_1 (MX-61[12]), pow_dac_r_1 (MX-61[11]). And the four digital volume controls are also separately controlled by vol_dac1_l (MX-19[15:8]), vol_dac1_r (MX-19[7:0]), vol_dac2_l (MX-1A[15:8] and vol_dac2_r (MX-1A[7:0]).

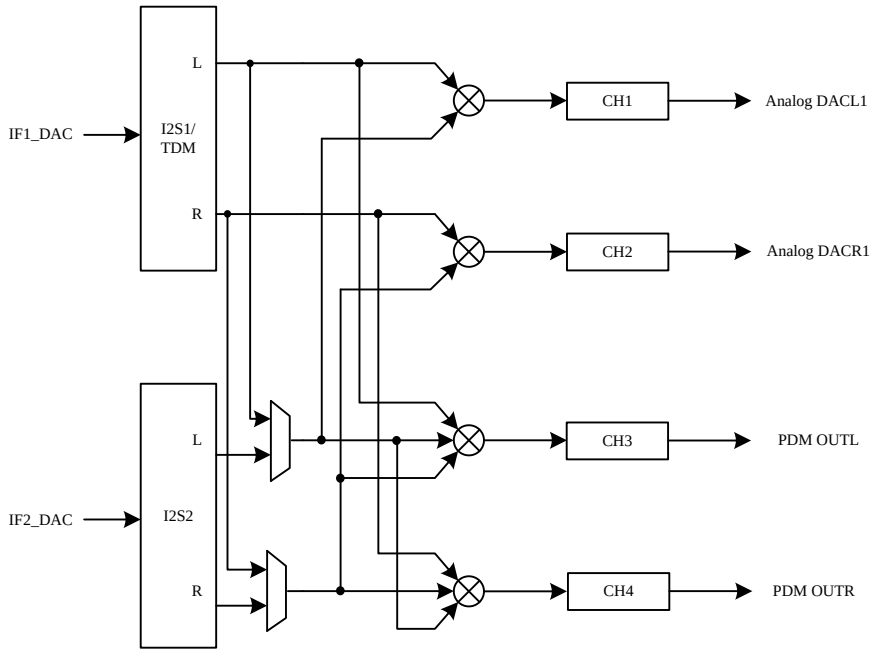


Figure 22. 4-Channel Playback Path

7.6.3. Mixers

The ALC5651 has digital and analog mixers build-in.

- **Output mixer - OUTMIXL/R**

  The stereo analog mixer can do mixing for DAC output and analog input. The mixer output is mainly for headphone output and line output. Each input path has it's mute control to the mixer block in MX-4D ~ MX-52. pow_outmixl and pow_outmixr can be used to power on/off OUTMIXL/R

- **Record mixer – RECMIXL/R**

  The stereo analog mixer can do mixing for analog input and OUTMIX output. The mixer output is for ADC input. Each input path has it's mute control to the mixer block in MX-3B ~ MX-3E. pow_recmixl and pow_recmixr can be used to power on/off RECMIXL/R.

- **Digital mixer**

  There are 8 digital mixers in ALC5651. Four digital mixers are assigned for ADC recording. These four mixers can mix analog line input, analog microphone input and digital microphone input then output to I2S/TDM interface to other device. Another two digital mixers are assigned DAC playback. These mixers can mix digital data from I2S/TDM interface or ADC data from external analog signal. The mixed data is output to analog DAC and output port to drive external device. The other two mixers are use for DA-AD processing. The incoming data from I2S/TDM interface (DACDAT1) uses the two digital mixers to do mixing and output to another I2S interface (ADCDAT2).

7.7. Analog Audio Input Port

The ALC5651 has two types analog input ports: microphone input and line input.

- **IN1P**

  The IN1P is a microphone type input port. The input port is single-ended type input. The microphone input port has its microphone bias and microphone boost. The low noise microphone bias can improve recording performance and enhance recording quality. Build-in short current detection scheme can be used for switch detection. Multi-steps microphone boost gain set by sel_bst1 (MX-0D[15:12]) is easy to use for microphone application. Pow_bst1 can be used to power down the MIC1 boost and pow_micbias1 can be used to power down the microphone bias 1.

- **IN2P/N**

  The IN2P/N is a dual type input port: microphone input and line input. Microphone input can be configured to differential input or single-ended input by MX-0D[6]. Multi-steps microphone boost gain set by sel_bst2 (MX-0D[11:8]) is easy to use for microphone application. Pow_bst2 can be used to power down the MIC2 boost. As line input, it has volume control for tuning by MX-0F[12:8] and MX-0F[4:0].

- **IN3P**

  The IN3P is a microphone type input port. The input port is single-ended type input. The microphone input port has its microphone bias and microphone boost. The low noise microphone bias can improve recording performance and enhance recording quality. Build-in short current detection scheme can be used for switch detection. Multi-steps microphone boost gain set by sel_bst1 (MX-0D[15:12]) is easy to use for microphone application. Pow_bst1 can be used to power down the MIC1 boost.

7.8. Analog Audio Output Port

The ALC5651 supports two type output ports:

- **HPO_L/R**

  The headphone output of ALC5651 is a stereo output with cap-free type headphone amplifier. It does not need to connect external capacitor and can connect to earphone device directly. The headphone output source can mix from output mixer (OUTMIX) or DAC by setting MX-45. The front stage of headphone output has volume control and gain control. The volume range is from +12dB to -46.5dB with 1.5dB/step by MX-02.
  En_l_hp and en_r_hp (MX-63[7/6]) can be used to power on/off Headphone Amplifier, and pow_hpo_voll and pow_hpo_volr (MX-66[11/10]) can be used to power on/off headphone volume control. In addition, pow_pump_hp (MX-8E[3]) can be used to power on/off charge pump circuit for Headphone Amplifier.

- **Line_OUT_L/R/P/N**

  The output type is line type output. The output is a stereo single ended output or mono differential output. The input can be selected from OUTVOL or DAC output by setting MX-53[15:12]. The front stage of LOUT output has gain control for attenuation. The gain control is 0dB or -6dB by MX-53[11].

7.9. Multi-Function Pins

There are five multi-function pins in ALC5651. For different functions in each pins are controlled by register. You need to set the right register settings for each multi-function pins by your application.

- **GPIO1/IRQ – Pin 37**

The pin default is GPIO function. If want to change to IRQ output, write MX-C0[15] to 1'b that will switch to IRQ function.

- **GPIO2/DMIC_SCL – Pin 38**

The pin default is GPIO function. If want to change to DMIC clock output, write MX-C0[14] to 1'b that will switch to DMIC clock output function.

- **IN1P/DMIC_DAT – Pin 4**

The pin default is DMIC data input function. In DMIC data input function, need to set these register settings:

1. Power down IN1P – MX-64[15] = 0'b
2. Mute IN1 to each analog mixer - (RECMIXL/RECMIXR/OUTMIXL/OUTMIXR).
3. Set MX-64[5] = 1'b
4. Select DMIC data input port, MX-75[11:10] = 01'b
5. Power on DMIC interface, MX-75[15] = 1'b

- **IN2N/JD2 – Pin 6**

In IN2N microphone input function, need to disable JD2 jack detection function – MX-64[1] = 0'b.

In JD2 jack detection function, need to set these register settings:

1. Power on JD2 – MX-64[1] = 1'b
2. Mute IN2 to each analog mixer - (RECMIXL/RECMIXR/OUTMIXR).
3. Set MX-64[4] = 1'b
4. Enable JD2 as jack detection source – MX-BC[11:9] = 011'b

- **LRCK2/BCLK2 – Pin 28/29**

These two pins can share with GPIO function by MX-C0[8]. "0'b" for I2S pin function and "1'b" for GPIO function.

- **ADCDAT2 – Pin 26**

The pin can configure to GPIO function or DMIC data input function by MX-C0[8] and MX-C0[6].

- **DACDAT2 – Pin 27**

The pin can configure to GPIO function or IRQ output function by MX-C0[8] and MX-C0[7].

- **PDM_SDA – Pin 24**

The pin can configure to PDM interface function, GPIO function or IRQ output function by MX-C0[3] and MX-C0[5].

- **PDM_SCL – Pin 25**

The pin can configure to PDM interface function, GPIO function or DMIC data input function by MX-C0[3] and MX-C0[4].

7.10. DRC and AGC Function

The Dynamic Range Controller (DRC) dynamically adjusts the input signal and let the output signal achieve the target level. The ALC5651 supports playback DRC for DAC path, and the DRC can also be used as AGC(Auto Gain Controller) for ADC path. The control register is at MX-B4[15:14]. The function block is shown as below. The signal input pass through the Pre-Gain first, then DRC volume and Post-Gain then output. The Pre-Gain is use to enlarge the input signal. The DRC volume is use to attenuate the signal after detected by DRC. The Post-Gain is use to fine tune the signal after pass DRC tuning.

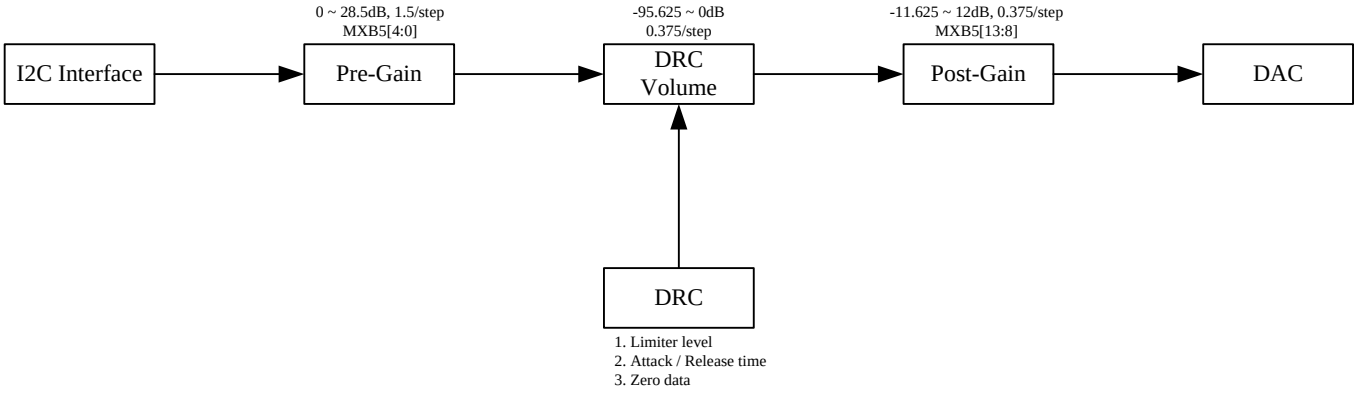


Figure 23. DAC DRC Function Block

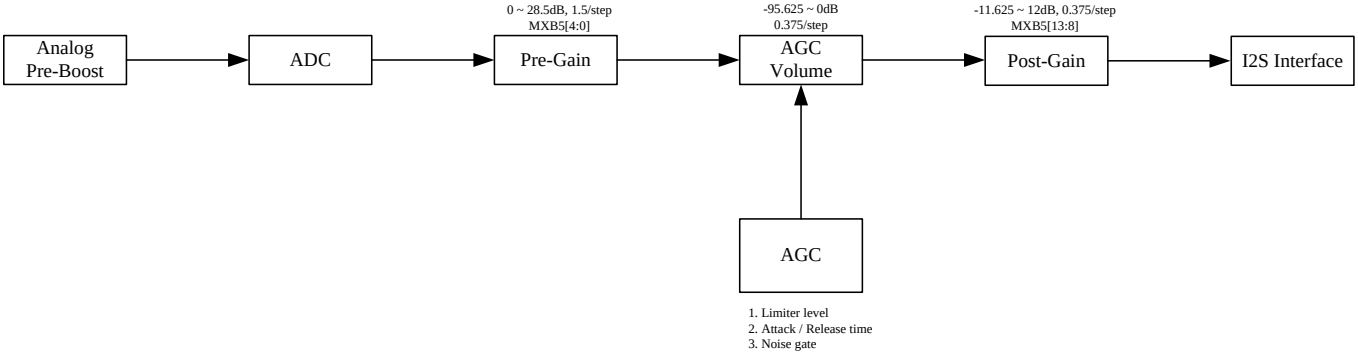


Figure 24. ADC AGC Function Block

Playback/Recording Mode:

For DAC playback or ADC recording mode, when the input signal exceeds target threshold, the signal will decrease "DRC/AGC Digital Volume" (0.375dB/step at every zero-crossing) until drop to target level then keep the digital volume. When input signal is below the target threshold, the signal will step-up "DRC/AGC Digital Volume" (0.375dB/step every zero-crossing) until return to original level. If want to return to the target level, need to set the pre-gain to achieve.

Fine tune parameters:

- Limiter Threshold: 0 ~ -46.5dB, 1.5dB/step, MX-B6[11:7]
- Attack Rate: T=(4*2^n)/sample rate, n = MX-B4[12:8]
- Recovery Rate: T=(4*2^n)/sample rate, n = MX-B4[4:0]

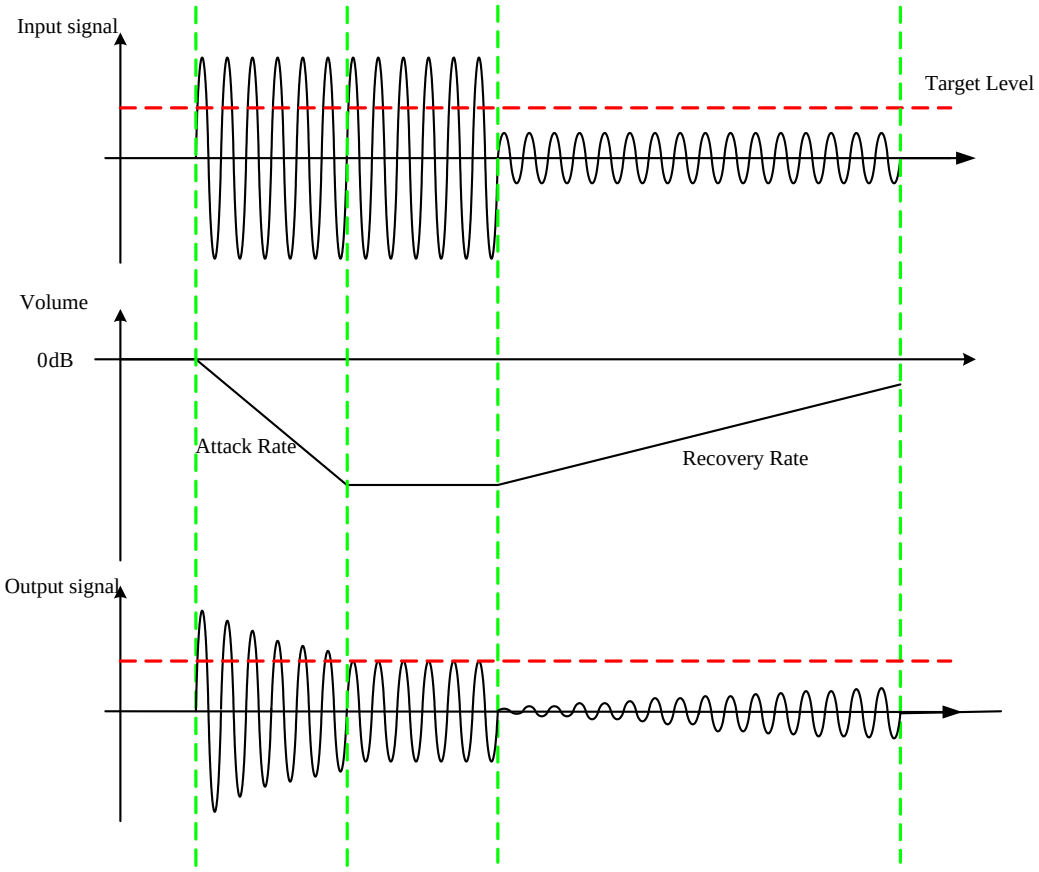


Figure 25. DRC/AGC for Playback/Recording Mode

Noise Gate Mode:

The Noise Gate Function is use to reduce the noise floor for DAC path or ADC path. When input signal is below noise gate level, the input signal will be reduced by DRC/AGC volume in order to suppress the background noise. The reducing level can be set by register. And when input signal is above noise gate, the input signal will be boosted to target level.

Fine tune parameters:

- Noise Gate Threshold: -36 ~ -82.5dB, 1.5dB/step, MX-B6[4:0]
- Noise Gate Attack Rate: T=(4*2^n)/sample rate, n = PR-06[4:0]
- Noise Gate Recovery Rate: T=(4*2^n)/sample rate, n = PR-02[12:8]
- Reducing Noise Level: 0 ~ 45dB, 3dB/step, MX-B6[15:12]

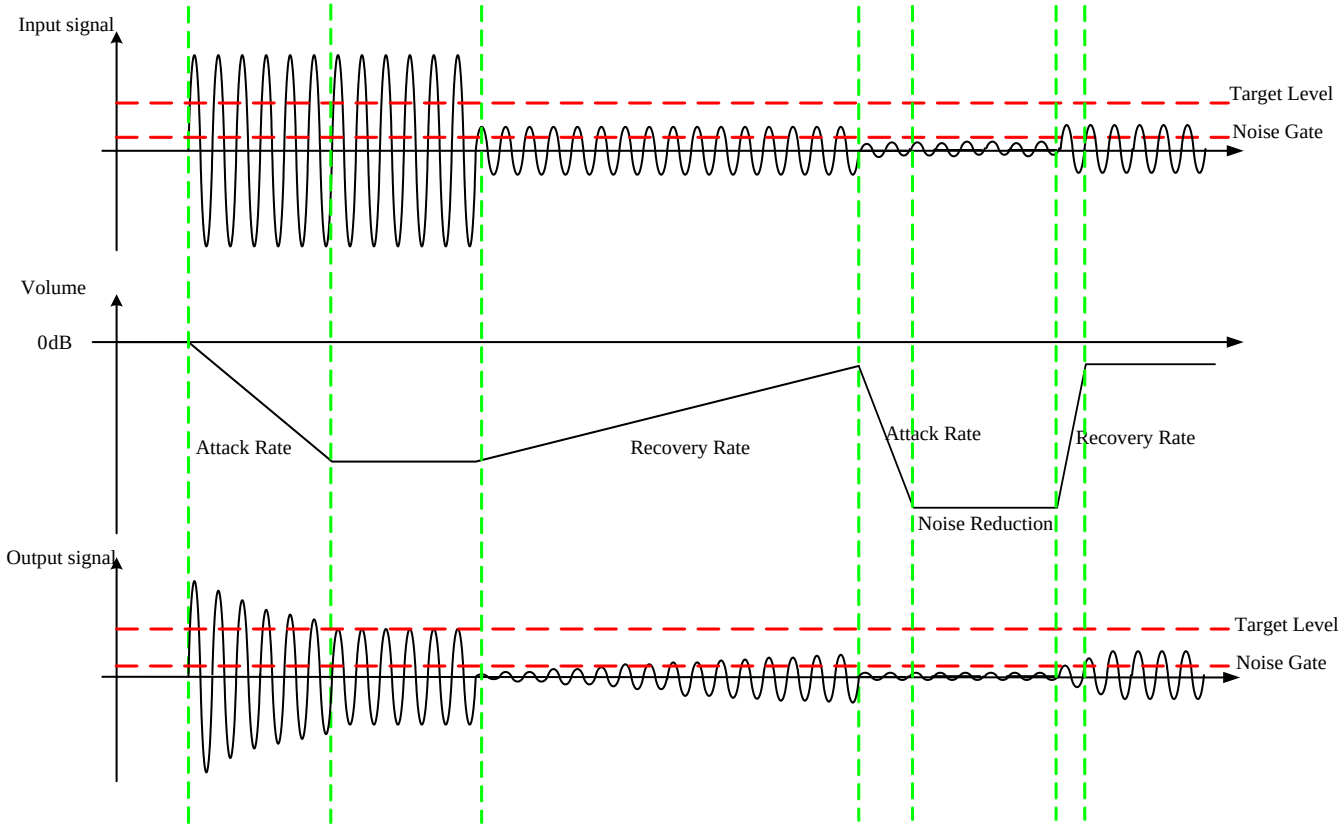


Figure 26. DRC/AGC for Noise Gate Mode

7.11. SounzReal Sound Effect

The Realtek's SounzReal sound effect is composed of:

- OmniSound
- Dipole Speaker
- TruTreble
- BassBack

7.12. Equalizer Block

The equalizer block cascades 7 bands of equalizer to tailor the frequency characteristics of embedded speaker system according to user preferences and to emulate environment sound. The 7 bands equalizer includes two high pass filter, four band pass filter and one low pass filter. One high pass filter cascaded in the front end is used to drop low frequency tone, The tone has a large amplitude and may damage a mini speaker. The high pass filter can be used to adjust Treble strength with gain control. One low pass filter with gain control can adjust the Bass strength. Four bands of bi-quad band pass filters are used to emulate environment sounds, e.g., 'Pub', 'Live', 'Rock',… etc.. The gain, center frequency and bandwidth of each filter are all programmable.

7.13. Wind Filter with Dynamic Wind Noise Detector

7.13.1. Wind Filter

The wind filter is implemented by a high pass filter. The wind filter is mainly for ADC recording used. The cut-off frequency of wind filter is programmable and is varied according to different sample rate. The filter is used to remove DC offset at normal condition, and to remove wind noise at application mode.

Wind filter setting procedure:

Step1: Disable wind filter – MX-D3[15]

Step2: Select target sample rate – MX-D3[14:12] and MX-D3[10:8]

Step3: Fine tune wind filter Fc – MX-D4[13:8] and MX-D4[5:0]

Step4: Enable wind filter – MX-D3[15]

The following table is shown the Fc with sample rate selection.
For the formula of Fc calculation is also shown as:

$Fc = (Fs * \tan^{-1}(a/(2-a))) / \pi$

Where:
Sample rate = 8K/12K/16K (MX-D3[14:12] & [10:8]), $a = 2^{-6} + n * 2^{-6}$ (n is MX-D4[13:8] & [5:0])
Sample rate = 24K/32K (MX-D3[14:12] & [10:8]), $a = 2^{-7} + n * 2^{-7}$ (n is MX-D4[13:8] & [5:0])
Sample rate = 44.1K/48L (MX-D3[14:12] & [10:8]), $a = 2^{-8} + n * 2^{-8}$ (n is MX-D4[13:8] & [5:0])
Sample rate = 88.2K/96L (MX-D3[14:12] & [10:8]), $a = 2^{-9} + n * 2^{-9}$ (n is MX-D4[13:8] & [5:0])
Sample rate = 176.4K/192L (MX-D3[14:12] & [10:8]), $a = 2^{-10} + n * 2^{-10}$ (n is MX-D4[13:8] & [5:0])

Table 13. Sample Rate with filter coefficient for Wind Filter

MX-D4	L & R Channel Sample Rate Setting				
n	8K	16K	32K	44.1K	48K
000000’b, 0	20.0	40.1	39.9	27.4	29.8
000001’b, 1	40.4	80.8	80.2	55.0	59.9
000010’b, 2	61.1	122.2	120.7	82.7	90.0
000011’b, 3	82.1	164.2	161.6	110.5	120.3
000100’b, 4	103.4	206.9	202.8	138.4	150.6
000101’b, 5	125.1	250.2	244.4	166.4	181.1
000110’b, 6	147.1	294.3	286.2	194.5	211.7
000111’b, 7	169.5	339.0	328.4	222.7	242.5
001000’b, 8	192.2	384.4	371.0	251.1	273.3
001001’b, 9	215.2	430.5	413.8	279.5	304.3
001010’b, 10	238.7	477.4	457.0	308.1	335.4
001011’b, 11	262.4	524.9	500.5	336.8	366.6
001100’b, 12	286.6	573.2	544.4	365.6	397.9
001101’b, 13	311.1	622.3	588.6	394.5	429.4
001110’b, 14	336.0	672.1	633.2	423.5	460.9
001111’b, 15	361.3	722.6	678.1	452.6	492.6
010000’b, 16	386.9	773.9	723.3	481.9	524.5
010001’b, 17	413.0	826.0	768.9	511.2	556.4
010010’b, 18	439.4	878.9	814.9	540.7	588.5
010011’b, 19	466.2	932.5	861.2	570.3	620.7
010100’b, 20	493.5	987.0	907.8	600.0	653.0
010101’b, 21	521.1	1042.2	954.9	629.8	685.5
010110’b, 22	549.1	1098.2	1002.2	659.7	718.1
010111’b, 23	577.5	1155.0	1050.0	689.8	750.8
011000’b, 24	606.3	1212.7	1098.1	719.9	783.6
011001’b, 25	635.5	1271.1	1146.6	750.2	816.6
011010’b, 26	665.1	1330.3	1195.5	780.6	849.6
011011’b, 27	695.2	1390.4	1244.7	811.1	882.9
011100’b, 28	725.6	1451.2	1294.3	841.8	916.2
011101’b, 29	756.4	1512.9	1344.3	872.5	949.7
011110’b, 30	787.6	1575.3	1394.7	903.4	983.3
011111’b, 31	819.3	1638.6	1445.4	934.4	1017.0
100000’b, 32	851.3	1702.7	1496.5	965.5	1050.9
100001’b, 33	883.7	1767.5	1548.0	996.8	1084.9
100010’b, 34	916.6	1822.3	1599.9	1028.1	1119.0
100011’b, 35	949.8	1899.6	1652.2	1059.6	1153.3
100100’b, 36	983.3	1966.7	1704.9	1091.2	1187.7

MX-D4 n	L & R Channel Sample Rate Setting				
	8K	16K	32K	44.1K	48K
100101’b, 37	1017.3	2034.7	1757.9	1122.9	1222.2
100110’b, 38	1051.6	2103.3	1811.4	1154.8	1256.9
100111’b, 39	1086.3	2172.7	1865.2	1186.7	1291.7
101000’b, 40	1121.4	2242.9	1919.5	1218.8	1326.6
101001’b, 41	1156.8	2313.7	1974.1	1251.0	1361.7
101010’b, 42	1192.6	2385.2	2029.1	1283.4	1396.9
101011’b, 43	1228.7	2457.4	2084.6	1315.8	1432.2
101100’b, 44	1265.1	2530.2	2140.4	1348.4	1467.7
101101’b, 45	1301.8	2603.6	2196.6	1381.1	1503.3
101110’b, 46	1338.8	2677.7	2253.3	1414.0	1539.0
101111’b, 47	1376.1	2752.3	2310.3	1447.0	1574.9
110000’b, 48	1413.7	2827.5	2367.7	1480.0	1610.9
110001’b, 49	1451.5	2903.1	2425.5	1513.3	1647.1
110010’b, 50	1489.6	2979.3	2483.8	1546.6	1683.4
110011’b, 51	1528.0	3056.0	2542.4	1580.1	1719.8
110100’b, 52	1566.5	3133.1	2601.5	1613.7	1756.4
110101’b, 53	1605.3	3210.6	2660.9	1647.4	1793.1
110110’b, 54	1644.2	3288.4	2720.8	1681.3	1830.0
110111’b, 55	1683.3	3366.6	2781.0	1715.3	1867.0
111000’b, 56	1722.5	3445.1	2841.7	1749.4	1904.1
111001’b, 57	1761.9	3523.9	2902.7	1783.6	1941.4
111010’b, 58	1801.4	3602.9	2964.2	1818.0	1978.8
111011’b, 59	1841.0	3682.1	3026.1	1852.5	2016.3
111100’b, 60	1880.7	3761.4	3088.3	1887.1	2054.0
111101’b, 61	1920.4	3840.8	3151.0	1921.9	2091.9
111110’b, 62	1960.2	3920.4	3214.1	1956.8	2129.9
111111’b, 63	2000.0	4000.0	3277.5	1991.8	2168.0

7.14. I²C Control Interface

I²C is a 2-wire (SCL/SDA) half-duplex serial communication interface, supporting only slave mode. SCL is used for clock and SDA is for data. SCL clock supports up to 400KHz rate and SDA data is a open drain structure. The input has built-in spike filter and can remove less than 50ns spike at SCL and SDA.

7.14.1. Address Setting

Table 14. Address Setting (0x34h)

(MSB)			BIT				(LSB)
0	0	1	1	0	1	0	R/W

7.14.2. Complete Data Transfer

Data Transfer over I²C Control Interface

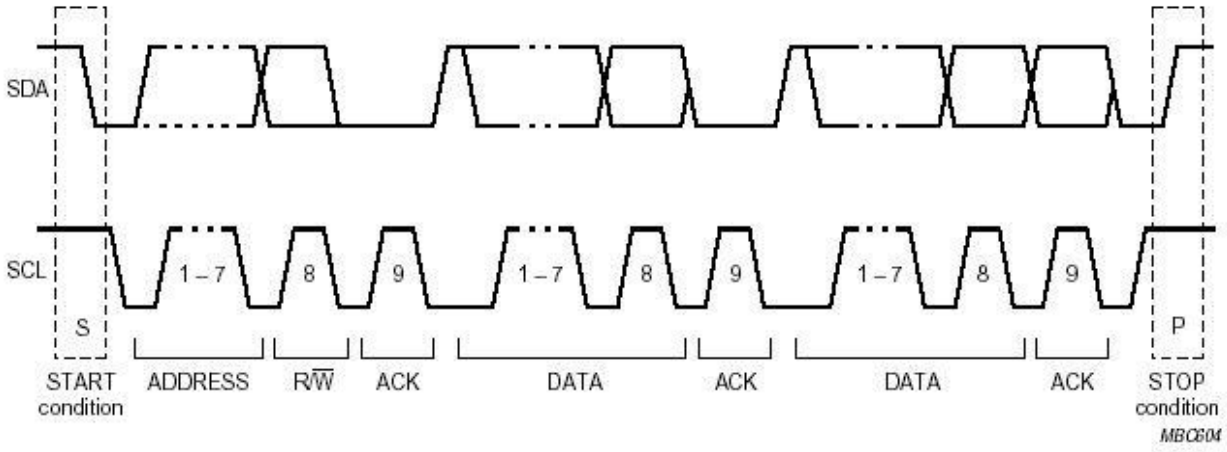
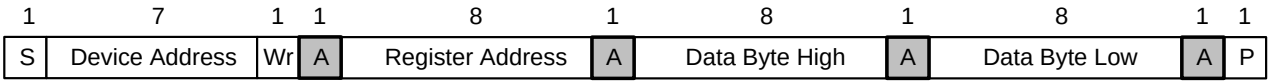


Figure 27. Data Transfer Over I²C Control Interface

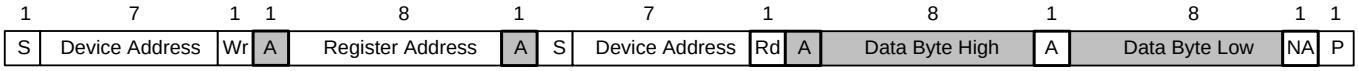
Write WORD Protocol

Table 15. Write WORD Protocol



Read WORD Protocol

Table 16. Read WORD Protocol



S: Start Condition
Slave Address: 7-bit Device Address
Wr: 0 for Write Command
Rd: 1 for Read Command
Command Code: 8-bit Register Address

A: 0 for ACK, 1 for NACK
Data Byte: 16-bit Mixer data
□: Master-to-Slave
□: Slave-to-Master

7.15. GPIO, Interrupt and Jack Detection

The ALC5651 supports 8 GPIOs – GPIO1 ~ GPIO8. There are 6 GPIOs (GPIO1 ~ GPIO6) can be configured to jack detection pins. For jack detection purpose, it needs switch GPIO to input pin.

For GPIO function, the GPIO can be configured to input or output. For input type, the internal circuit can read pin status and report to register table. For output type, the internal circuit can drive this pin to high or low to control external device. In GPIO function, the pin polarity can be controlled by register at output type.

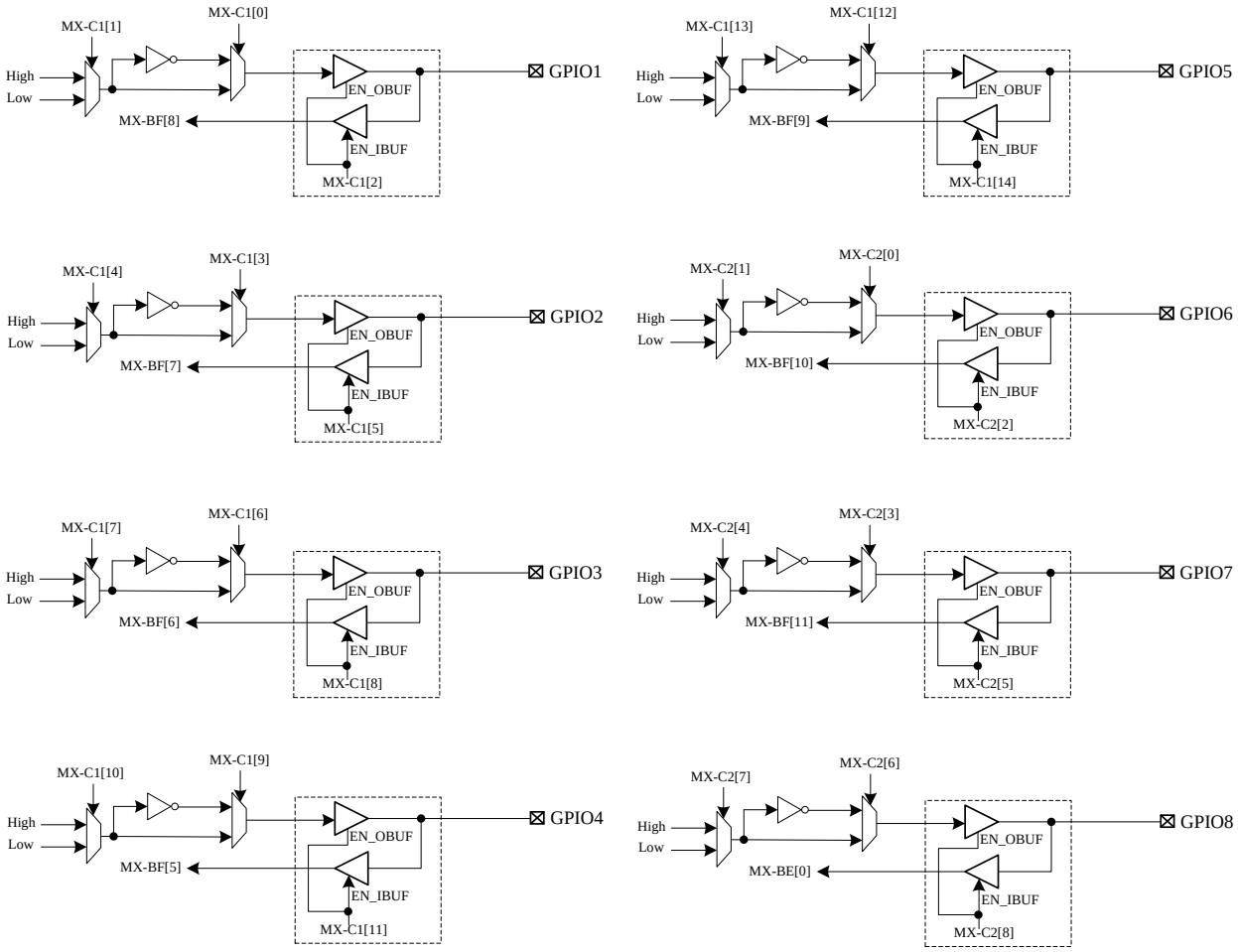


Figure 28. GPIO Function Block

For IRQ function is shown at Figure 28, the IRQ output source can be selected from gpio_jd Status, jd1_1 Status, jd1_2 Status, jd2 Status and MICBIAS1 Over-Current Status. When either status is trigged, the GPIO will output a flag as interrupt signal to external device.

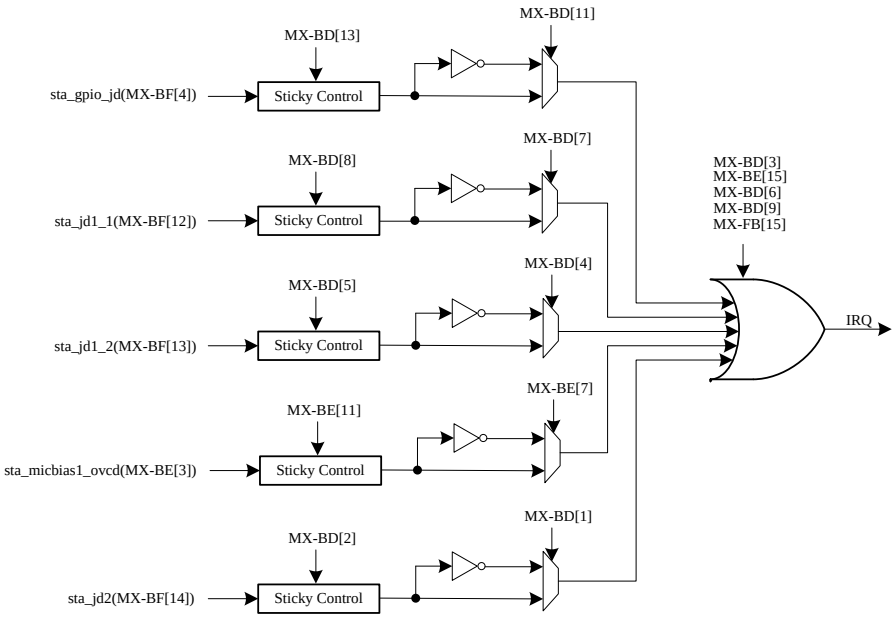
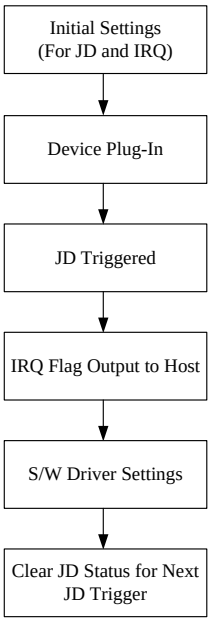


Figure 29. IRQ Function Block

In general, the IRQ output needs to combine with JD function. When JD is trigger, IRQ will output a flag to host to notice S/W driver. The S/W driver will do something by system design. The behavior flow chard as following:



The MICBIAS supports short detection function. When MICBIAS circuit is short, MICBIAS circuit will generate an over-current flag. The flag can generate an interrupt signal to notice host and let S/W do follow-up processes.

For jack detection pins are shown at Figure 29. There are 6 GPIOs pins can be selected and control by MX-BB[15:13]. When has GPIOs been triggered, the status sta_jd_internal – MX-BF[4] will change. JD1 pin can used to detect two jacks and has two statuses for each jack. JD2 pin only used to detection one jack.

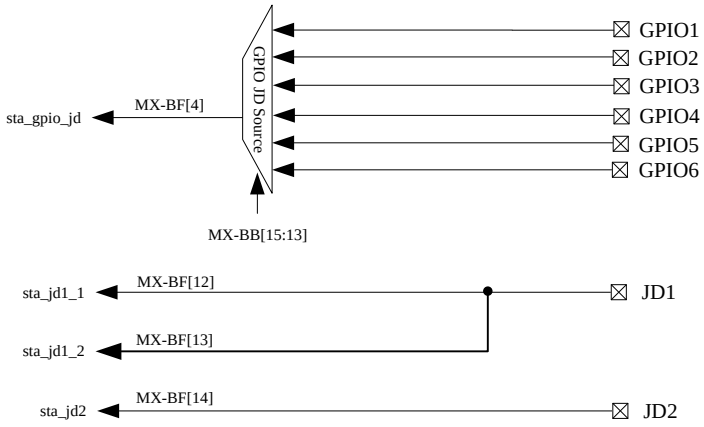


Figure 30. JD Source Selection

The jack detect function can be used to turn-on or turn-off the related output ports. When jack detect pin is trigged, the selected output ports will turn-on or turn-off. For example on HP and LOUT auto switch when JD is trigger.

Setting procedure:

1. Select JD source: use sta_jd1_1 as JD status. MX-BC[11:9] = 001’b
2. Set target behavior by JD active – HP & LOUT auto switch when JD is triggered.
   MX-BB[11:10] = 11’b & MX-BB[3:2] = 10’b
3. When JD status is low, HP_OUT is mute and LOUT is un-mute.
   When JD status is low go high, HP is un-mute and LOUT is mute.

Note: For HP and SPK jack switch function, driver need to turn-on DAC to HP path and DAC to LOUT path first. The register control of MX-BB is only do mute/un-mute function for HP and SPK.

7.16. Power Management

ALC5651 detailed Power Management control registers are supported in MX-61h, 62h, 63h, 64h, 65h and 66h. Each particular block will only be active when each bit of each register is set to enable.

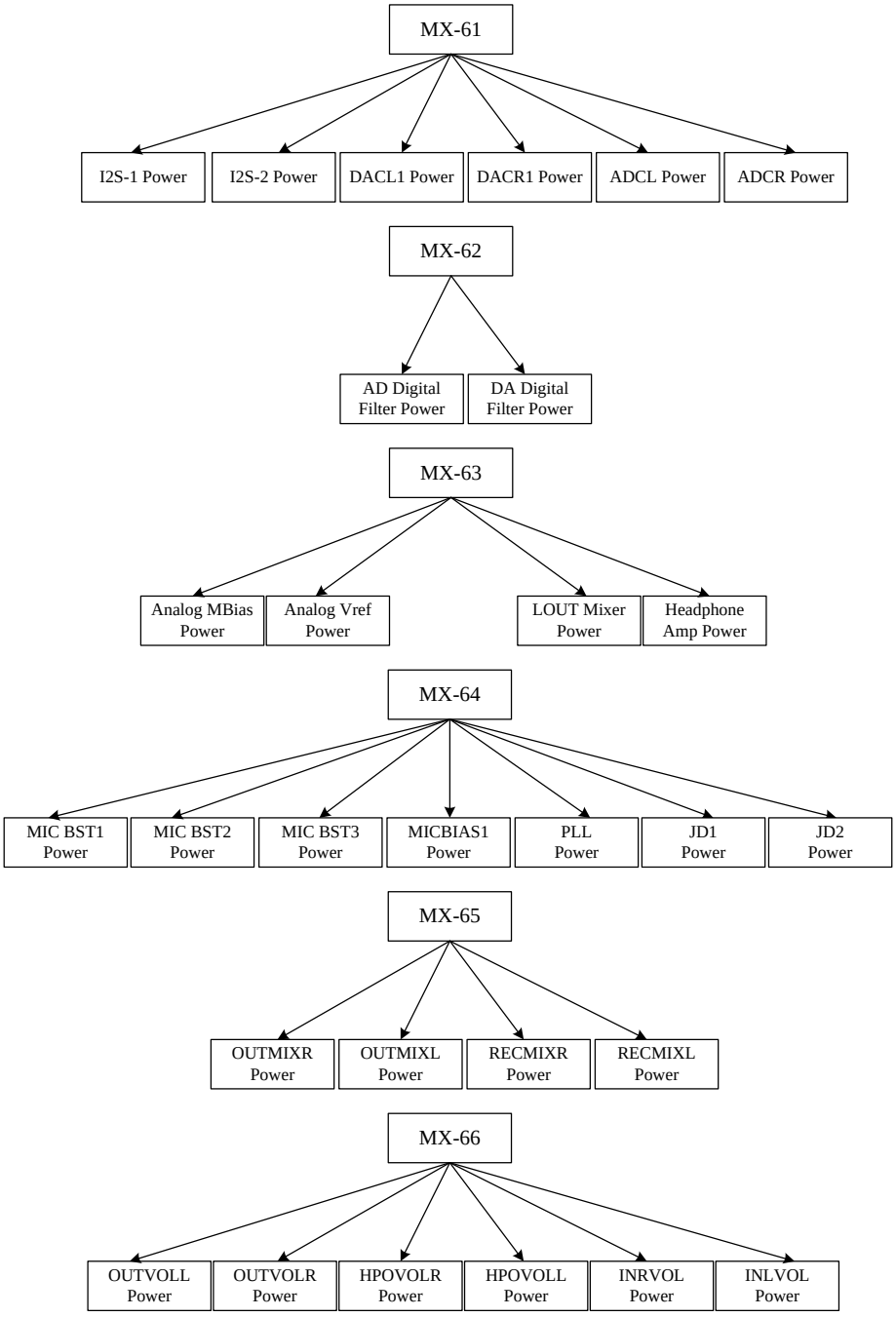


Figure 31. Power Management

7.17. PDM Interface

The ALC5651 supports one PDM interface for drive external PDM amplifiers. There are two wires for this interface, one is serial PDM clock and the other is serial PDM data. Except for transmit PDM data, it also can transmit command pattern for control external PDM amplifier. The PDM command pattern is 8-bit length pattern and can selected 64-times repeat or 128-times repeat for different PDM amplifier vendor. The command pattern format is shown as:

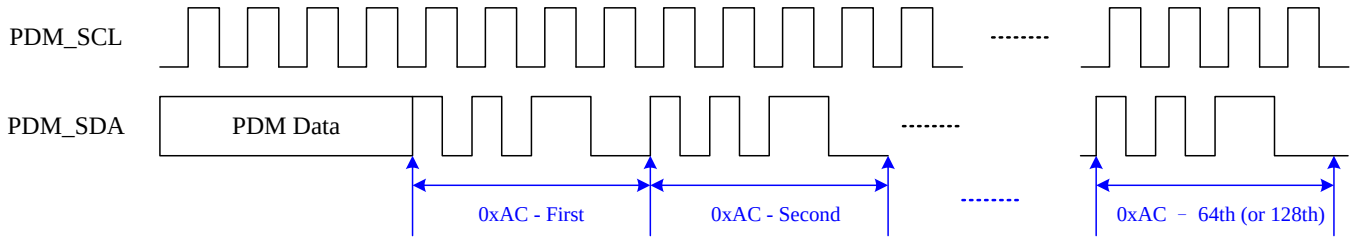


Figure 32. PDM Command Pattern Format

8. Registers List

ALC5651 register map as shown as following and accessing unimplemented registers will return a 0.

8.1. Register Map

Table 17. Register Map

Type	Name	Description	Register Address	Reset State
Reset	S/W Reset	S/W Reset & Device ID	MX-00h	0x0000'h
	HPOUT	Headphone Output Volume & Mute/Un-Mute	MX-02h	0xC8C8'h
	Line Output	Line Output Control 1	MX-03h	0xC8C8'h
		Line Output Control 2	MX-05h	0x0000'h
	MIC Input	IN1/2 Mode and Gain Boost Control	MX-0Dh	0x0000'h
		IN3 Mode and Gain Boost Control	MX-0Eh	0x0000'h
	Line Input	INL/INR Volume Control	MX-0Fh	0x0808'h
Digital Gain/Volume	DACL1/R1	DACL1/R1 Digital Volume Control	MX-19h	0xAFAF'h
	DACL2/R2-1	DACL2/R2 Digital Volume Control	MX-1Ah	0xAFAF'h
	DACL2/R2-2	DACL2/R2 Digital Mute/Un-Mute Control	MX-1Bh	0x0C00'h
	ADCL/R-1	ADCL/R Digital Volume & Mute/Un-Mute Control	MX-1Ch	0x2F2F'h
	ADCL/R-2	ADCL/R Digital Path Volume Control	MX-1Dh	0x2F2F'h
	ADCL/R-3	ADC Boost Gain for DMIC	MX-1Eh	0x0000'h
Digital Mixer	ADC-1	ADC Stereo1 Digital Mixer Control	MX-27h	0x7860'h
	ADC-2	ADC Stereo2 Digital Mixer Control	MX-28h	0x7070'h
	ADC-3	ADC to DAC Digital Mixer Control	MX-29h	0x8080'h
	DAC-1	DAC Stereo Digital Mixer Control	MX-2Ah	0x5252'h
	DAC-2	DD Digital Mixer Control	MX-2Bh	0x5454'h
	Copy Mode	ADC/DAC Data Copy Mode Control	MX-2Fh	0x0000'h
PDM Output	PDM	PDM Output Control	MX-30h	0x5000'h
		PDM Command Control 1	MX-31h	0x0000'h
		PDM Command Control 2	MX-32h	0x0000'h
Input Mixer	RECMIXL-1	RECMIXL Gain Control	MX-3Bh	0x0000'h
	RECMIXL-2	RECMIXL Gain & Selection Control	MX-3Ch	0x006F'h
	RECMIXR-1	RECMIXR Gain Control	MX-3Dh	0x0000'h
	RECMIXR-2	RECMIXR Gain & Selection Control	MX-3Eh	0x006F'h
Output Mixer	HPOMIX	HPOMIX Gain & Selection Control	MX-45h	0x6000'h
	OUTMIXL-1	OUTMIXL Control 1	MX-4Dh	0x0000'h
	OUTMIXL-2	OUTMIXL Control 2	MX-4Eh	0x0000'h
	OUTMIXL-3	OUTMIXL Control 3	MX-4Fh	0x0279'h
	OUTMIXR-1	OUTMIXR Control 1	MX-50h	0x0000'h
	OUTMIXR-2	OUTMIXR Control 2	MX-51h	0x0000'h
	OUTMIXR-3	OUTMIXR Control 3	MX-52h	0x0279'h
	LOUTMIX	LOUTMIX Control	MX-53h	0xF000'h
Power Management	Management-1	I2S & DAC & ADC & Power Control	MX-61h	0x0000'h
	Management-2	Digital Filter, PDM Power Control	MX-62h	0x0000'h
	Management-3	VREF & MBias & LOUTMIX & HP & LDO Power Control	MX-63h	0x00C0'h
	Management-4	MICBST & MICBIAS & JD Power Control	MX-64h	0x0000'h

Type	Name	Description	Register Address	Reset State
	Management-5	OUTMIX & RECMIX Power Control	MX-65h	0x0000'h
	Management-6	OUTVOL & HPOVOL & INVOL Power Control	MX-66h	0x0000'h
PR Register	PR Index	PR Register Index	MX-6Ah	0x0000'h
	PR Data	PR Register Data	Mx-6Ch	0x0000'h
Digital Interface	I2S1 Port Ctrl	I2S-1 Interface Control	MX-70h	0x8000'h
	I2S2 Port Ctrl	I2S-2 Interface Control	MX-71h	0x8000'h
	ADC/DAC Clock-1	ADC/DAC Clock Control-1	MX-73h	0x1104'h
	ADC/DAC Clock-2	ADC/DAC Clock Control-2	MX-74h	0x0C00'h
Digital MIC	DMIC	Digital Microphone Control	MX-75h	0x1400'h
TDM Interface	TDM	TDM Interface Control 1	MX-77h	0x0C00'h
		TDM Interface Control 2	MX-78h	0x4000'h
		TDM Interface Control 3	MX-79h	0x0123'h
Global Clock	Global Clock	Global Clock Control	MX-80h	0x0000'h
	PLL-1	PLL Control-1	MX-81h	0x0000'h
	PLL-2	PLL Control-2	MX-82h	0x0000'h
	ASRC-1	ASRC Control-1	MX-83h	0x0800'h
	ASRC-2	ASRC Control-2	MX-84h	0x0000'h
	ASRC-3	ASRC Control-3	MX-85h	0x0008'h
	ASRC-4	ASRC Control-4	MX-89h	0x0000'h
HP Amp	HP	HP Amp Control 1	MX-8Eh	0x0004'h
		HP Amp Control 2	MX-8Fh	0x1100'h
MICBIAS	MICBIAS	MICBIAS Control	MX-93h	0x2000'h
JD	JD	Jack Detection Control	MX-94h	0x0200'h
EQ	EQ-1	EQ Control-1	MX-B0h	0x2080'h
	EQ-2	EQ Control-2	MX-B1h	0x0000'h
	EQ-Parameter	EQ Low Pass Filter – a1	PR-A0h	0x1C10'h
	EQ-Parameter	EQ Low Pass Filter – H0	PR-A1h	0x01F4'h
	EQ-Parameter	EQ Band Pass Filter 1 – a1	PR-A2h	0xC5E9'h
	EQ-Parameter	EQ Band Pass Filter 1 – a2	PR-A3h	0x1A98'h
	EQ-Parameter	EQ Band Pass Filter 1 – H0	PR-A4h	0x1D2C'h
	EQ-Parameter	EQ Band Pass Filter 2 – a1	PR-A5h	0xC882'h
	EQ-Parameter	EQ Band Pass Filter 2 – a2	PR-A6h	0x1C10'h
	EQ-Parameter	EQ Band Pass Filter 2 – H0	PR-A7h	0x01F4'h
	EQ-Parameter	EQ Band Pass Filter 3 – a1	PR-A8h	0xE904'h
	EQ-Parameter	EQ Band Pass Filter 3 – a2	PR-A9h	0x1C10'h
	EQ-Parameter	EQ Band Pass Filter 3 – H0	PR-AAh	0x01F4'h
	EQ-Parameter	EQ Band Pass Filter 4 – a1	PR-ABh	0xE904'h
	EQ-Parameter	EQ Band Pass Filter 4 – a2	PR-ACh	0x1C10'h
	EQ-Parameter	EQ Band Pass Filter 4 – H0	PR-ADh	0x01F4'h
	EQ-Parameter	EQ High Pass Filter 1 – a1	PR-AEh	0x1C10'h
	EQ-Parameter	EQ High Pass Filter 1 – H0	PR-AFh	0x01F4'h
	EQ-Parameter	EQ High Pass Filter 2 – a1	PR-B0h	0x2000'h
	EQ-Parameter	EQ High Pass Filter 2 – a2	PR-B1h	0x0000'h
	EQ-Parameter	EQ High Pass Filter 2 – H0	PR-B2h	0x2000'h
DRC/AGC	DRC/AGC-1	DRC/AGC Control-1	MX-B4h	0x2206'h
	DRC/AGC-2	DRC/AGC Control-2	MX-B5h	0x1F00'h
	DRC/AGC-3	DRC/AGC Control-3	MX-B6h	0x0000'h

Type	Name	Description	Register Address	Reset State
Jack Detection	JD-1	Jack Detection Control-1	MX-BBh	0x0000'h
	JD-2	Jack Detection Control-2	MX-BCh	0x0000'h
IRQ	IRQ-1	IRQ Control-1	MX-BDh	0x0000'h
	IRQ-2	IRQ Control-2	MX-BEh	0x0000'h
Flag Status	Status	GPIO & Internal Status	MX-BFh	0x0000'h
GPIO	GPIO-1	GPIO Control-1	MX-C0h	0x0100'h
	GPIO-2	GPIO Control-2	MX-C1h	0x0000'h
	GPIO-3	GPIO Control-3	MX-C2h	0x0000'h
SounzReal Sound Effect	BassBack	BassBack Control	MX-CFh	0x0013'h
	TruTreble	TruTreble Control-1	MX-D0h	0x0680'h
	TruTreble	TruTreble Control-2	MX-D1h	0x1C17'h
	OmniSound	OmniSound Control	PR-63h	0x3717'h
Wind Filter	Control-1	Wind Filter Control 1	MX-D3h	0xB320'h
	Control-2	Wind Filter Control 2	MX-D4h	0x0000'h
SVOL & ZCD	SVOL & ZCD	Soft Volume and ZCD Control	MX-D9h	0x0809'h
General Control		General Control 1	MX-FAh	0x0010'h
		ADC/DAC RESET Control	PR-3Dh	0x2800'h
Vendor ID	ID	Vendor ID	MX-FEh	0x10EC'h

8.2. MX-00h: S/W Reset & Device ID

Default: 0000’h

Table 18. MX-00h: S/W Reset & Device ID

Port Name	Bits	Read/Write	Reset State	Description
Reserved	15:6	R	0’h	Reserved
Device_id	5	R	0’h	ALC5651
Reserved	4:0	R	0’h	Reserved

Note: Writes to this register will reset all registers to their default values.

8.3. MX-02h: Headphone Output Control

Default: C8C8’h

Table 19. MX-02h: Headphone Output Control

Name	Bits	Read/Write	Reset State	Description
mu_hpo_l	15	R/W	1’h	Mute Control for Left Headphone Output Port (HPOL) 0’b: Un-Mute 1’b: Mute
Mu_hpovoll_in	14	R/W	1’h	Mute Control for Left Headphone Volume Channel (HPOVOLL) 0’b: Un-Mute 1’b: Mute
vol_hpol	13:8	R/W	8’h	Left Headphone Channel Volume Control (HPOVOLL) ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step
mu_hpo_r	7	R/W	1’h	Mute Control Right Headphone Output Port (HPOR) 0’b: Un-Mute 1’b: Mute
Mu_hpovolr_in	6	R/W	1’h	Mute Control for Right Headphone Volume Channel (HPOVOLR) 0’b: Un-Mute 1’b: Mute

Name	Bits	Read/Write	Reset State	Description
Vol_hpor	5:0	R/W	8'h	Right Headphone Channel Volume Control (HPOVOLR)❶ 00'h: +12dB … 08'h: 0dB … 27'h: -46.5dB, with 1.5dB/step

❶Volume Table

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12	32	20	-36
1	1	10.5	17	11	-13.5	33	21	-37.5
2	2	9	18	12	-15	34	22	-39
3	3	7.5	19	13	-16.5	35	23	-40.5
4	4	6	20	14	-18	36	24	-42
5	5	4.5	21	15	-19.5	37	25	-43.5
6	6	3	22	16	-21	38	26	-45
7	7	1.5	23	17	-22.5	39	27	-46.5
8	8	0	24	18	-24			
9	9	-1.5	25	19	-25.5			
10	A	-3	26	1A	-27			
11	B	-4.5	27	1B	-28.5			
12	C	-6	28	1C	-30			
13	D	-7.5	29	1D	-31.5			
14	E	-9	30	1E	-33			
15	F	-10.5	31	1F	-34.5			

8.4. MX-03h: LINE Output Control 1

Default: C8C8’h

Table 20. MX-03h: LINE Output Control 1

Name	Bits	Read/Write	Reset State	Description
Mu_lout_l	15	R/W	1’h	Mute Control for Left Line Output Port(LOUTL) 0’b: Un-Mute 1’b: Mute
Mu_outvoll_in	14	R/W	1’h	Mute Control for Left Output Volume Channel (OUTVOLL) 0’b: Un-Mute 1’b: Mute
Vol_outl	13:8	R/W	08’h	Left Output Volume Control (OUTVOLL) ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step
Mu_lout_r	7	R/W	1’h	Mute Control for Right Line Output Port (LOUTR) 0’b: Un-Mute 1’b: Mute
Mu_outvolr_in	6	R/W	1’h	Mute Control for Right Output Volume Channel (OUTVOLR) 0’b: Un-Mute 1’b: Mute
Vol_outr	5:0	R/W	08’h	Right Output Volume Control ❶ 00’h: +12dB … 08’h: 0dB … 27’h: -46.5dB, with 1.5dB/step

❶Volume Table

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12	32	20	-36
1	1	10.5	17	11	-13.5	33	21	-37.5
2	2	9	18	12	-15	34	22	-39
3	3	7.5	19	13	-16.5	35	23	-40.5
4	4	6	20	14	-18	36	24	-42
5	5	4.5	21	15	-19.5	37	25	-43.5
6	6	3	22	16	-21	38	26	-45
7	7	1.5	23	17	-22.5	39	27	-46.5
8	8	0	24	18	-24			
9	9	-1.5	25	19	-25.5			

10	A	-3	26	1A	-27			
11	B	-4.5	27	1B	-28.5			
12	C	-6	28	1C	-30			
13	D	-7.5	29	1D	-31.5			
14	E	-9	30	1E	-33			
15	F	-10.5	31	1F	-34.5			

8.5. MX-05h: LINE Output Control 2

Default: 0000'h

Table 21. MX-05h: LINE Output Control 2

Name	Bits	Read/Write	Reset State	Description
En_dfo	15	R/W	0'h	Enable Differential Line Output 0'b: Disable 1'b: Enable (LP / RN)
reserved	14:0	R	0'h	Reserved

8.6. MX-0Dh: IN1/2 Input Control

Default: 0000'h

Table 22. MX-0Dh: IN1/2 Input Control

Name	Bits	Read/Write	Reset State	Description
Sel_bst1	15:12	R/W	0'h	IN1 Boost Control (BST1) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved

Name	Bits	Read/Write	Reset State	Description
Sel_bst2	11:8	R/W	0'h	IN2 Boost Control (BST2) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved
Reserved	7	R/W	0'h	Reserved
En_in2_df	6	R/W	0'h	IN2 Input Mode Control 0'b: Single Ended Mode 1'b: Differential Mode
reserved	5:0	R/W	0'h	Reserved

8.7. MX-0Eh: IN3 Input Control

Default: 0000'h

Table 23. MX-0Eh: IN3 Input Control

Name	Bits	Read/Write	Reset State	Description
Sel_bst3	15:12	R/W	0'h	IN3 Boost Control (BST3) 0000'b: Bypass 0001'b: +20dB 0010'b: +24dB 0011'b: +30dB 0100'b: +35dB 0101'b: +40dB 0110'b: +44dB 0111'b: +50dB 1000'b: +52dB Others : Reserved
Reserved	11:0	R	0'h	Reserved

8.8. MX-0Fh: INL & INR Volume Control

Default: 0808’h

Table 24. MX-0Fh: INL & INR Volume Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R	0’h	Reserved
Vol_inl	12:8	R/W	8’h	INL Channel Volume Control ❶ 00’h: +12dB … 08’h: 0dB … 1F’h: -34.5dB, with 1.5dB/step
Reserved	7:5	R	0’h	Reserved
Vol_inr	4:0	R/W	8’h	INR Channel Volume Control ❶ 00’h: +12dB … 08’h: 0dB … 1F’h: -34.5dB, with 1.5dB/step

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	12	16	10	-12
1	1	10.5	17	11	-13.5
2	2	9	18	12	-15
3	3	7.5	19	13	-16.5
4	4	6	20	14	-18
5	5	4.5	21	15	-19.5
6	6	3	22	16	-21
7	7	1.5	23	17	-22.5
8	8	0	24	18	-24
9	9	-1.5	25	19	-25.5
10	A	-3	26	1A	-27
11	B	-4.5	27	1B	-28.5
12	C	-6	28	1C	-30
13	D	-7.5	29	1D	-31.5
14	E	-9	30	1E	-33
15	F	-10.5	31	1F	-34.5

8.9. MX-19h: DACL1/R1 Digital Volume

Default: AFAF'h

Table 25. MX-19h: DACL1/R1 Digital Volume

Name	Bits	Read/Write	Reset State	Description
vol_dac1_l	15:8	R/W	AF'h	DAC1 Left Channel Digital Volume 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step
vol_dac1_r	7:0	R/W	AF'h	DAC1 Right Channel Digital Volume 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step

8.10. MX-1Ah: DACL2/R2 Digital Volume

Default: AFAF'h

Table 26. MX-1Ah: DACL2/R2 Digital Volume

Name	Bits	Read/Write	Reset State	Description
vol_dac2_l	15:8	R/W	AF'h	DAC2 Left Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step
vol_dac2_r	7:0	R/W	AF'h	DAC2 Right Channel Digital Volume❶ 00'h: -65.625dB … AF'h: 0dB, with 0.375dB/Step

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-65.625	53	35	-45.75	106	6A	-25.875	159	9F	-6	212	D4	
1	1	-65.25	54	36	-45.375	107	6B	-25.5	160	A0	-5.625	213	D5	
2	2	-64.875	55	37	-45	108	6C	-25.125	161	A1	-5.25	214	D6	
3	3	-64.5	56	38	-44.625	109	6D	-24.75	162	A2	-4.875	215	D7	
4	4	-64.125	57	39	-44.25	110	6E	-24.375	163	A3	-4.5	216	D8	
5	5	-63.75	58	3A	-43.875	111	6F	-24	164	A4	-4.125	217	D9	
6	6	-63.375	59	3B	-43.5	112	70	-23.625	165	A5	-3.75	218	DA	

7	7	-63	60	3C	-43.125	113	71	-23.25	166	A6	-3.375	219	DB	
8	8	-62.625	61	3D	-42.75	114	72	-22.875	167	A7	-3	220	DC	
9	9	-62.25	62	3E	-42.375	115	73	-22.5	168	A8	-2.625	221	DD	
10	A	-61.875	63	3F	-42	116	74	-22.125	169	A9	-2.25	222	DE	
11	B	-61.5	64	40	-41.625	117	75	-21.75	170	AA	-1.875	223	DF	
12	C	-61.125	65	41	-41.25	118	76	-21.375	171	AB	-1.5	224	E0	
13	D	-60.75	66	42	-40.875	119	77	-21	172	AC	-1.125	225	E1	
14	E	-60.375	67	43	-40.5	120	78	-20.625	173	AD	-0.75	226	E2	
15	F	-60	68	44	-40.125	121	79	-20.25	174	AE	-0.375	227	E3	
16	10	-59.625	69	45	-39.75	122	7A	-19.875	175	AF	0	228	E4	
17	11	-59.25	70	46	-39.375	123	7B	-19.5	176	B0		229	E5	
18	12	-58.875	71	47	-39	124	7C	-19.125	177	B1		230	E6	
19	13	-58.5	72	48	-38.625	125	7D	-18.75	178	B2		231	E7	
20	14	-58.125	73	49	-38.25	126	7E	-18.375	179	B3		232	E8	
21	15	-57.75	74	4A	-37.875	127	7F	-18	180	B4		233	E9	
22	16	-57.375	75	4B	-37.5	128	80	-17.625	181	B5		234	EA	
23	17	-57	76	4C	-37.125	129	81	-17.25	182	B6		235	EB	
24	18	-56.625	77	4D	-36.75	130	82	-16.875	183	B7		236	EC	
25	19	-56.25	78	4E	-36.375	131	83	-16.5	184	B8		237	ED	
26	1A	-55.875	79	4F	-36	132	84	-16.125	185	B9		238	EE	
27	1B	-55.5	80	50	-35.625	133	85	-15.75	186	BA		239	EF	
28	1C	-55.125	81	51	-35.25	134	86	-15.375	187	BB		240	F0	
29	1D	-54.75	82	52	-34.875	135	87	-15	188	BC		241	F1	
30	1E	-54.375	83	53	-34.5	136	88	-14.625	189	BD		242	F2	
31	1F	-54	84	54	-34.125	137	89	-14.25	190	BE		243	F3	
32	20	-53.625	85	55	-33.75	138	8A	-13.875	191	BF		244	F4	
33	21	-53.25	86	56	-33.375	139	8B	-13.5	192	C0		245	F5	
34	22	-52.875	87	57	-33	140	8C	-13.125	193	C1		246	F6	
35	23	-52.5	88	58	-32.625	141	8D	-12.75	194	C2		247	F7	
36	24	-52.125	89	59	-32.25	142	8E	-12.375	195	C3		248	F8	
37	25	-51.75	90	5A	-31.875	143	8F	-12	196	C4		249	F9	
38	26	-51.375	91	5B	-31.5	144	90	-11.625	197	C5		250	FA	
39	27	-51	92	5C	-31.125	145	91	-11.25	198	C6		251	FB	
40	28	-50.625	93	5D	-30.75	146	92	-10.875	199	C7		252	FC	
41	29	-50.25	94	5E	-30.375	147	93	-10.5	200	C8		253	FD	
42	2A	-49.875	95	5F	-30	148	94	-10.125	201	C9		254	FE	

43	2B	-49.5	96	60	-29.625	149	95	-9.75	202	CA		255	FF	
44	2C	-49.125	97	61	-29.25	150	96	-9.375	203	CB				
45	2D	-48.75	98	62	-28.875	151	97	-9	204	CC				
46	2E	-48.375	99	63	-28.5	152	98	-8.625	205	CD				
47	2F	-48	100	64	-28.125	153	99	-8.25	206	CE				
48	30	-47.625	101	65	-27.75	154	9A	-7.875	207	CF				
49	31	-47.25	102	66	-27.375	155	9B	-7.5	208	D0				
50	32	-46.875	103	67	-27	156	9C	-7.125	209	D1				
51	33	-46.5	104	68	-26.625	157	9D	-6.75	210	D2				
52	34	-46.125	105	69	-26.25	158	9E	-6.375	211	D3				

8.11. MX-1Bh: DACL2/R2 Mute/Un-Mute Control

Default: 0C00’h

Table 27. MX-1Bh: DACL2/R2 Mute/Un-Mute Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0’h	Reserved
Mu_dac2_l	13	R/W	0’h	Mute Control for Left DAC2 Volume 0’b: Un-Mute 1’b: Mute
Mu_dac2_r	12	R/W	0’h	Mute Control for Right DAC2 Volume 0’b: Un-Mute 1’b: Mute
Sel_dacl2	11	R/W	1’h	Select IF1 or IF2 Data to DACL2 0’b: IF1_DAC_L 1’b: IF2_DAC_L
Sel_dacr2	10	R/W	1’h	Select IF1 or IF2 Data to DACR2 0’b: IF1_DAC_R 1’b: IF2_DAC_R
reserved	9:0	R	0’h	Reserved

8.12. MX-1Ch: Stereo1 ADC Digital Volume Control

Default: 2F2F'h

Table 28. MX-1Ch: Stereo1 ADC Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
Mu_adc_vol_l	15	R/W	0'h	Mute Control for Stereo1 ADC Left Volume Channel 0'b: Un-Mute 1'b: Mute
Vol_adc1_l	14:8	R/W	2F'h	Stereo1 ADC Left Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step
Mu_adc_vol_r	7	R/W	0'h	Mute Control for Stereo1 ADC Right Volume Channel 0'b: Un-Mute 1'b: Mute
Vol_adc1_r	6:0	R/W	2F'h	Stereo1 ADC Right Channel Volume Control 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step

8.13. MX-1Dh: Stereo2 ADC Digital Volume Control

Default: 2F2F'h

Table 29. MX-1Dh: Stereo2 ADC Digital Volume Control

Name	Bits	Read/Write	Reset State	Description
Mu_adc2_vol_l	15	R/W	0'h	Digital Mute For Stereo2 ADC Left Channel Digital Mixer 0'b: Un-Mute 1'b: Mute
Vol_adc2_l	14:8	R/W	2F'h	Stereo2 ADC Left Channel Volume Control ❶ 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step
Mu_adc2_vol_r	7	R/W	0'h	Digital Mute For Stereo2 ADC Right Channel Digital Mixer 0'b: Un-Mute 1'b: Mute
Vol_adc2_r	6:0	R/W	2F'h	Stereo2 ADC Right Channel Volume Control ❶ 00'h: -17.625dB … 2F'h: 0dB … 7F'h: +30dB, with 0.375dB/Step

❶Volume Table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-17.625	26	1A	-7.875	52	34	1.875	78	4E	11.625	104	68	21.375
1	1	-17.25	27	1B	-7.5	53	35	2.25	79	4F	12	105	69	21.75
2	2	-16.875	28	1C	-7.125	54	36	2.625	80	50	12.375	106	6A	22.125
3	3	-16.5	29	1D	-6.75	55	37	3	81	51	12.75	107	6B	22.5
4	4	-16.125	30	1E	-6.375	56	38	3.375	82	52	13.125	108	6C	22.875
5	5	-15.75	31	1F	-6	57	39	3.75	83	53	13.5	109	6D	23.25
6	6	-15.375	32	20	-5.625	58	3A	4.125	84	54	13.875	110	6E	23.625
7	7	-15	33	21	-5.25	59	3B	4.5	85	55	14.25	111	6F	24
8	8	-14.625	34	22	-4.875	60	3C	4.875	86	56	14.625	112	70	24.375
9	9	-14.25	35	23	-4.5	61	3D	5.25	87	57	15	113	71	24.75
10	A	-13.875	36	24	-4.125	62	3E	5.625	88	58	15.375	114	72	25.125
11	B	-13.5	37	25	-3.75	63	3F	6	89	59	15.75	115	73	25.5
12	C	-13.125	38	26	-3.375	64	40	6.375	90	5A	16.125	116	74	25.875
13	D	-12.75	39	27	-3	65	41	6.75	91	5B	16.5	117	75	26.25
14	E	-12.375	40	28	-2.625	66	42	7.125	92	5C	16.875	118	76	26.625

15	F	-12	41	29	-2.25	67	43	7.5	93	5D	17.25	119	77	27
16	10	-11.625	42	2A	-1.875	68	44	7.875	94	5E	17.625	120	78	27.375
17	11	-11.25	43	2B	-1.5	69	45	8.25	95	5F	18	121	79	27.75
18	12	-10.875	44	2C	-1.125	70	46	8.625	96	60	18.375	122	7A	28.125
19	13	-10.5	45	2D	-0.75	71	47	9	97	61	18.75	123	7B	28.5
20	14	-10.125	46	2E	-0.375	72	48	9.375	98	62	19.125	124	7C	28.875
21	15	-9.75	47	2F	0	73	49	9.75	99	63	19.5	125	7D	29.25
22	16	-9.375	48	30	0.375	74	4A	10.125	100	64	19.875	126	7E	29.625
23	17	-9	49	31	0.75	75	4B	10.5	101	65	20.25	127	7F	30
24	18	-8.625	50	32	1.125	76	4C	10.875	102	66	20.625			
25	19	-8.25	51	33	1.5	77	4D	11.25	103	67	21			

8.14. MX-1Eh: ADC Digital Boost Gain Control

Default: 0000’h

Table 30. MX-1Eh: ADC Digital Boost Gain Control

Name	Bits	Read/Write	Reset State	Description
Ad_boost_gain_l	15:14	R/W	0’h	ADC Left Channel Digital Boost Gain 00’b: 0dB 01’b: 12dB 10’b: 24dB 11’b: 36dB
Ad_boost_gain_r	13:12	R/W	0’h	ADC Right Channel Digital Boost Gain 00’b: 0dB 01’b: 12dB 10’b: 24dB 11’b: 36dB
reserved	11:0	R/W	0’h	Reserved

8.15. MX-27h: Stereo1 ADC Digital Mixer Control

Default: 7860'h

Table 31. MX-27h: Stereo1 ADC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	reserved
mu_stereo1_adcl1	14	R/W	1'h	Mute Control for Stereo1 ADC1 Left Channel 0'b: Un-Mute 1'b: Mute
mu_stereo1_adcl2	13	R/W	1'h	Mute Control for Stereo1 ADC2 Left Channel 0'b: Un-Mute 1'b: Mute
sel_stereo1_adc1	12	R/W	1'h	Select Control for Stereo1 ADC1 Source 0'b: DD_MIXL/ DD_MIXR 1'b: ADCL/ADCR
sel_stereo1_adc2	11	R/W	1'h	Select Control for Stereo1 ADC2 Source 0'b: DMIC_L/ DMIC_R 1'b: DD_MIXL/ DD_MIXR
reserved	10:7	R	0'h	Reserved
mu_stereo1_adcr1	6	R/W	1'h	Mute Control for Stereo1 ADC1 Right Channel 0'b: Un-Mute 1'b: Mute
mu_stereo1_adcr2	5	R/W	1'h	Mute Control for Stereo1 ADC2 Right Channel 0'b: Un-Mute 1'b: Mute
reserved	4:0	R	0'h	reserved

8.16. MX-28h: Stereo2 ADC Digital Mixer Control

Default: 7070'h

Table 32. MX-28h: Stereo2 ADC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	reserved
mu_stereo2_adcl1	14	R/W	1'h	Mute Control for Stereo2 ADC1 Left Channel 0'b: Un-Mute 1'b: Mute
mu_stereo2_adcl2	13	R/W	1'h	Mute Control for Stereo2 ADC2 Left Channel 0'b: Un-Mute 1'b: Mute
sel_stereo2_adcl1	12	R/W	1'h	Select Control for Stereo2 ADC1 Left Channel Source 0'b: DD_MIXL 1'b: ADCL
sel_stereo2_adcl2	11	R/W	0'h	Select Control for Stereo2 ADC2 Left Channel Source 0'b: DMIC_L 1'b: DD_MIXL
reserved	10:7	R	0'h	reserved

Name	Bits	Read/Write	Reset State	Description
mu_stereo2_adcr1	6	R/W	1'h	Mute Control for Stereo2 ADC1 Right Channel 0'b: Un-Mute 1'b: Mute
mu_stereo2_adcr2	5	R/W	1'h	Mute Control for Stereo2 ADC2 Right Channel 0'b: Un-Mute 1'b: Mute
sel_stereo2_adcr1	4	R/W	1'h	Select Control for Stereo2 ADC1 Right Channel Source 0'b: DD_MIXR 1'b: ADCR
sel_stereo2_adcr2	3	R/W	0'h	Select Control for Stereo2 ADC2 Right Channel Source 0'b: DMIC_R 1'b: DD_MIXR
reserved	2:0	R	0'h	Reserved

8.17. MX-29h: Stereo ADC to DAC Digital Mixer Control

Default: 8080'h

Table 33. MX-29h: Stereo ADC to DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
mu_stereo1_adc_mixer_l	15	R/W	1'h	Mute Control for Stereo1 ADC Left Channel to DAC 0'b: Un-Mute 1'b: Mute
mu_dac1_l	14	R/W	0'h	Mute Control for I2S-1 to DAC Left Channel 0'b: Un-Mute 1'b: Mute
Reserved	13:8	R	0'h	Reserved
mu_stereo1_adc_mixer_r	7	R/W	1'h	Mute Control for Stereo1 ADC Right Channel to DAC 0'b: Un-Mute 1'b: Mute
mu_dac1_r	6	R/W	0'h	Mute Control for I2S-1 to DAC Right Channel 0'b: Un-Mute 1'b: Mute
reserved	5:0	R	0'h	reserved

8.18. MX-2Ah: Stereo DAC Digital Mixer Control

Default: 5252’h

Table 34. MX-2Ah: Stereo DAC Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0’h	reserved
mu_stereo_dacl1_mixl	14	R/W	1’h	Mute Control for DACL1 to Stereo DAC Left Mixer 0’b: Un-Mute 1’b: Mute
gain_dacl1_to_stereo_l	13	R/W	0’h	Gain Control for DACL1 to Stereo DAC Left Mixer 0’b: 0dB 1’b: -6dB
mu_stereo_dacl2_mixl	12	R/W	1’h	Mute Control for DACL2 to Stereo DAC Left Mixer 0’b: Un-Mute 1’b: Mute
gain_dacl2_to_stereo_l	11	R/W	0’h	Gain Control for DACL2 to Stereo DAC Left Mixer 0’b: 0dB 1’b: -6dB
Reserved	10	R	0’h	reserved
mu_stereo_dacr1_mixl	9	R/W	1’h	Mute Control for DACR1 to Stereo DAC Left Mixer 0’b: Un-Mute 1’b: Mute
gain_dacr1_to_stereo_l	8	R/W	0’h	Gain Control for DACR1 to Stereo DAC Left Mixer 0’b: 0dB 1’b: -6dB
Reserved	7	R	0’h	reserved
mu_stereo_dacr1_mixr	6	R/W	1’h	Mute Control for DACR1 to Stereo DAC Right Mixer 0’b: Un-Mute 1’b: Mute
gain_dacr1_to_stereo_r	5	R/W	0’h	Gain Control for DACR1 to Stereo DAC Right Mixer 0’b: 0dB 1’b: -6dB
mu_stereo_dacr2_mixr	4	R/W	1’h	Mute Control for DACR2 to Stereo DAC Right Mixer 0’b: Un-Mute 1’b: Mute
gain_dacr2_to_stereo_r	3	R/W	0’h	Gain Control for DACR2 to Stereo DAC Right Mixer 0’b: 0dB 1’b: -6dB
reserved	2	R	0’h	reserved
mu_stereo_dacl1_mixr	1	R/W	1’h	Mute Control for DACL1 to Stereo DAC Right Mixer 0’b: Un-Mute 1’b: Mute
gain_dacl1_to_stereo_r	0	R/W	0’h	Gain Control for DACL1 to Stereo DAC Right Mixer 0’b: 0dB 1’b: -6dB

8.19. MX-2Bh: DD Digital Mixer Control

Default: 5454'h

Table 35. MX-2Bh: DD Digital Mixer Control

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
mu_stereo_dd_l1	14	R/W	1'h	Mute Control for DACL1 to DD Left Mixer 0'b: Un-Mute 1'b: Mute
gain_stereo_dd_l1	13	R/W	0'h	Gain Control for DACL1 to DD Left Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dd_l2	12	R/W	1'h	Mute Control for DACL2 to DD Left Mixer 0'b: Un-Mute 1'b: Mute
gain_stereo_dd_l2	11	R/W	0'h	Gain Control for DACL2 to DD Left Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dd_r2_l	10	R/W	1'h	Mute Control for DACR2 to DD Left Mixer 0'b: Un-Mute 1'b: Mute
gain_stereo_dd_r2_l	9	R/W	0'h	Gain Control for DACR2 to DD Left Mixer 0'b: 0dB 1'b: -6dB
reserved	8:7	R	0'h	Reserved
mu_stereo_dd_r1	6	R/W	1'h	Mute Control for DACR1 to DD Right Mixer 0'b: Un-Mute 1'b: Mute
gain_stereo_dd_r1	5	R/W	0'h	Gain Control for DACR1 to DD Right Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dd_r2	4	R/W	1'h	Mute Control for DACR2 to DD Right Mixer 0'b: Un-Mute 1'b: Mute
gain_stereo_dd_r2	3	R/W	0'h	Gain Control for DACR2 to DD Right Mixer 0'b: 0dB 1'b: -6dB
mu_stereo_dd_l2_r	2	R/W	1'h	Mute Control for DACL2 to DD Right Mixer 0'b: Un-Mute 1'b: Mute
gain_stereo_dd_l2_r	1	R/W	0'h	Gain Control for DACL2 to DD Right Mixer 0'b: 0dB 1'b: -6dB
reserved	0	R	0'h	reserved

8.20. MX-2Fh: Interface DAC/ADC Data Control

Default: 0000’h

Table 36. MX-2Fh: Interface DAC/ADC Data Control

Name	Bits	Read/Write	Reset State	Description
reserved	15:12	R	0’h	reserved
sel_if2_dac_data	11:10	R/W	0’h	Select Control for I2S2 DACDAT Data Location 00’b: Normal 01’b: Swap 10’b: Left Channel Copy to Right Channel 11’b: Right Channel Copy to Left Channel
sel_if2_adc_data	9:8	R/W	0’h	Select Control for I2S2 ADCDAT Data Location 00’b: Normal 01’b: Swap 10’b: Left Channel Copy to Right Channel 11’b: Right Channel Copy to Left Channel
Sel_if2_adc	7	R/W	0’h	Select IF2 ADCDAT Data Source 0’b: From IF1_ADC1 1’b: From IF1_ADC2
reserved	6:0	R	0’h	reserved

8.21. MX-30h: PDM Output Control

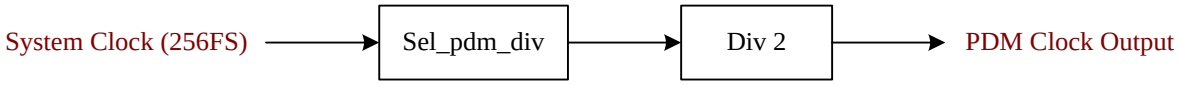
Default: 5000’h

Table 37. MX-30 PDM Output Control

Name	Bits	Read/Write	Reset Status	Description
sel_pdm_l	15	R/W	0’h	Select PDM Left channel source 0’b: DD_MIXL 1’b: Stereo_DAC_MIXL
mu_pdm_l	14	R/W	1’h	Mute PDM Left channel data 0’b: UnMute 1’b: Mute
sel_pdm_r	13	R/W	0’h	Select PDM Right channel source 0’b: DD_MIXR 1’b: Stereo_DAC_MIXR
mu_pdm_r	12	R/W	1’h	Mute PDM Right channel data 0’b: UnMute 1’b: Mute
reserved	11:7	R	0’h	Reserved
Pdm_cmd_busy	6	R	0’h	Pattern Controller Busy Flag 0’b: Normal 1’b: Busy
Sel_pdm_pattern_ctrl	5	R/W	0’h	Select Into PDM Pattern Control Repeat Count Number 0’b: Repeat 64 times (For ALC9010) 1’b: Repeat 128times (For SSM2517 and TFA9881)
Gain_pdm_in	4	R/W	0’h	PDM Gain Selection 0’b: -6dB 1’b: 0dB

Reserved	3:2	R	0’h	Reserved
Sel_pdm_div	1:0	R/W	0’h	System Clock to PDM Filter Divider ❶ 00’b: Div 1 01’b: Div 2 10’b: Div 3 11’b: Div 4

❶



8.22. MX-31h: PDM Command Control 1

Default: 0000’h

Table 38. MX-31 PDM Command Control 1

Name	Bits	Read / Write	Reset Status	Description
Reserved	15:12	R	0’h	Reserved
pdm_cmd_exe	11	R/W	0’h	Write “1” to Execute
Reserved	10:0	R	0’h	Reserved

8.23. MX-32h: PDM Command Control 21

Default: 0000’h

Table 39. MX-32 PDM Command Control 2

Name	Bits	Read / Write	Reset Status	Description
Reserved	15:8	R	0’h	Reserved
pdm_cmd_pattern	7:0	R/W	0’h	PDM Pattern Command

8.24. MX-3Bh: RECMIXL Control 1

Default: 0000’h

Table 40. MX-3Bh: RECMIXL Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R	0’h	reserved
Gain_inl_recmixl	12:10	R/W	0’h	Gain Control for INL to RECMIXL 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: Reserved
Reserved	9:7	R	0’h	Reserved

Name	Bits	Read/Write	Reset State	Description
Gain_bst3_recmixl	6:4	R/W	0'h	Gain Control for BST3 to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
Gain_bst2_recmixl	3:1	R/W	0'h	Gain Control for BST2 to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
reserved	0	R	0'h	reserved

8.25. MX-3Ch: RECMIXL Control 2

Default: 006F'h

Table 41. MX-3Ch: RECMIXL Control 2

Name	Bits	Read/Write	Reset State	Description
Gain_bst1_recmixl	15:13	R/W	0'h	Gain Control for BST1 to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
Gain_outmixl_recmixl	12:10	R/W	0'h	Gain Control for OUTMIXL to RECMIXL 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
reserved	9:6	R	1'h	reserved
Mu_inl_rexmixl	5	R/W	1'h	Mute Control for INL to RECMIXL 0'b: Un-Mute 1'b: Mute
reserved	4	R	0'h	reserved

Name	Bits	Read/Write	Reset State	Description
Mu_bst3_recmixl	3	R/W	1'h	Mute Control for BST3 to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst2_recmixl	2	R/W	1'h	Mute Control for BST2 to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_bst1_recmixl	1	R/W	1'h	Mute Control for BST1 to RECMIXL 0'b: Un-Mute 1'b: Mute
Mu_outmixl_recmixl	0	R/W	1'h	Mute Control for OUTMIXL to RECMIXL 0'b: Un-Mute 1'b: Mute

8.26. MX-3Dh: RECMIXR Control 1

Default: 0000'h

Table 42. MX-3Dh: RECMIXR Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R	0'h	Reserved
Gain_inr_recmixr	12:10	R/W	0'h	Gain Control for INR to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
reserved	9:7	R	0'h	Reserved
Gain_bst3_recmixr	6:4	R/W	0'h	Gain Control for BST3 to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
Gain_bst2_recmixr	3:1	R/W	0'h	Gain Control for BST2 to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
reserved	0	R	0'h	Reserved

8.27. MX-3Eh: RECMIXR Control 2

Default: 006F'h

Table 43. MX-3Eh: RECMIXR Control 2

Name	Bits	Read/Write	Reset State	Description
Gain_bst1_recmixr	15:13	R/W	0'h	Gain Control for BST1 to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
Gain_outmixr_recmixr	12:10	R/W	0'h	Gain Control for OUTMIXR to RECMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: Reserved
reserved	9:6	R	1'h	reserved
Mu_inr_rexmixr	5	R/W	1'h	Mute Control for INR to RECMIXR 0'b: Un-Mute 1'b: Mute
reserved	4	R	0'h	reserved
Mu_bst3_recmixr	3	R/W	1'h	Mute Control for BST3 to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst2_recmixr	2	R/W	1'h	Mute Control for BST2 to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst1_recmixr	1	R/W	1'h	Mute Control for BST1 to RECMIXR 0'b: Un-Mute 1'b: Mute
Mu_outmixr_recmixr	0	R/W	1'h	Mute Control for OUTMIXR to RECMIXR 0'b: Un-Mute 1'b: Mute

8.28. MX-45h: HPOMIX Control

Default: 6000’h

Table 44. MX-45h: HPOMIX Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0’h	Reserved
mu_dac1_hpomix	14	R/W	1’h	Mute Control for DAC1 to HPOMIX 0’b: Un-Mute 1’b: Mute
mu_hpovol_hpomix	13	R/W	1’h	Mute Control for HPOVOL to HPOMIX 0’b: Un-Mute 1’b: Mute
Gain_hpomix	12	R/W	0’h	Gain Control for HPOMIX 0’b: 0dB 1’b: -6dB
Reserved	11:0	R	0’h	Reserved

8.29. MX-4Dh: OUTMIXL Control 1

Default: 0000’h

Table 45. MX-4Dh: OUTMIXL Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R	0’h	Reserved
Gain_bst2_outmixl	12:10	R/W	0’h	Gain Control for BST2 to OUTMIXL 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Gain_bst1_outmixl	9:7	R/W	0’h	Gain Control for BST1 to OUTMIXL 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved

Name	Bits	Read/Write	Reset State	Description
Gain_inl_outmixl	6:4	R/W	0’h	Gain Control for INL to OUTMIXL 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Gain_recmixl_outmixl	3:1	R/W	0’h	Gain Control for RECMIXL to OUTMIXL 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
Reserved	0	R	0’h	reserved

8.30. MX-4Eh: OUTMIXL Control 2

Default: 0000’h

Table 46. MX-4Eh: OUTMIXL Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:10	R	0’h	Reserved
Gain_dacl1_outmixl	9:7	R/W	0’h	Gain Control for DACL1 to OUTMIXL 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved
reserved	6:0	R	0’h	Reserved

8.31. MX-4Fh: OUTMIXL Control 3

Default: 0279’h

Table 47. MX-4Fh: OUTMIXL Control 3

Name	Bits	Read/Write	Reset State	Description
reserved	15:7	R	4’h	Reserved
Mu_bst2_outmixl	6	R/W	1’h	Mute Control for BST2 to OUTMIXL 0’b: Un-Mute 1’b: Mute
Mu_bst1_outmixl	5	R/W	1’h	Mute Control for BST1 to OUTMIXL 0’b: Un-Mute 1’b: Mute
Mu_inl_outmixl	4	R/W	1’h	Mute Control for INL to OUTMIXL 0’b: Un-Mute 1’b: Mute
Mu_recmixl_outmixl	3	R/W	1’h	Mute Control for RECMIXL to OUTMIXL 0’b: Un-Mute 1’b: Mute
reserved	2:1	R	0’h	Reserved
Mu_dacl1_outmixl	0	R/W	1’h	Mute Control for DACL1 to OUTMIXL 0’b: Un-Mute 1’b: Mute

8.32. MX-50h: OUTMIXR Control 1

Default: 0000’h

Table 48. MX-50h: OUTMIXR Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:13	R	0’h	Reserved
Gain_bst2_outmixr	12:10	R/W	0’h	Gain Control for BST2 to OUTMIXR 000’b: 0dB 001’b: -3dB 010’b: -6dB 011’b: -9dB 100’b: -12dB 101’b: -15dB 110’b: -18dB Others: reserved

Name	Bits	Read/Write	Reset State	Description
Gain_bst1_outmixr	9:7	R/W	0'h	Gain Control for BST1 to OUTMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_inr_outmixr	6:4	R/W	0'h	Gain Control for INR to OUTMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
Gain_recmixr_outmixr	3:1	R/W	0'h	Gain Control for RECMIXR to OUTMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
reserved	0	R	0'h	Reserved

8.33. MX-51h: OUTMIXR Control 2

Default: 0000'h

Table 49. MX-51h: OUTMIXR Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:10	R	0'h	Reserved
Gain_dacr1_outmixr	9:7	R/W	0'h	Gain Control for DACR1 to OUTMIXR 000'b: 0dB 001'b: -3dB 010'b: -6dB 011'b: -9dB 100'b: -12dB 101'b: -15dB 110'b: -18dB Others: reserved
reserved	6:0	R	0'h	Reserved

8.34. MX-52h: OUTMIXR Control 3

Default: 0279'h

Table 50. MX-52h: OUTMIXR Control 3

Name	Bits	Read/Write	Reset State	Description
reserved	15:7	R	4'h	Reserved
Mu_bst2_outmixr	6	R/W	1'h	Mute Control for BST2 to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_bst1_outmixr	5	R/W	1'h	Mute Control for BST1 to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_inr_outmixr	4	R/W	1'h	Mute Control for INR to OUTMIXR 0'b: Un-Mute 1'b: Mute
Mu_recmixr_outmixr	3	R/W	1'h	Mute Control for RECMIXR to OUTMIXR 0'b: Un-Mute 1'b: Mute
Reserved	2:1	R	0'h	Reserved
Mu_dacr1_outmixr	0	R/W	1'h	Mute Control for DACR1 to OUTMIXR 0'b: Un-Mute 1'b: Mute

8.35. MX-53h: LOUTMIX Control

Default: F000'h

Table 51. MX-53h: LOUTMIX Control

Name	Bits	Read/Write	Reset State	Description
Mu_dacl1_lout	15	R/W	1'h	Mute Control for DACL1 to LOUTMIX 0'b: Un-Mute 1'b: Mute
Mu_dacr1_lout	14	R/W	1'h	Mute Control for DACR1 to LOUTMIX 0'b: Un-Mute 1'b: Mute
Mu_outvoll_lout	13	R/W	1'h	Mute Control for OUTVOLL to LOUTMIX 0'b: Un-Mute 1'b: Mute
Mu_outvolr_lout	12	R/W	1'h	Mute Control for OUTVOLR to LOUTMIX 0'b: Un-Mute 1'b: Mute
Gain_lout	11	R/W	0'h	Gain Control for LOUTMIX 0'b: 0dB 1'b: -6dB
reserved	10:0	R/W	0'h	Reserved

8.36. MX-61h: Power Management Control 1

Default: 0000'h

Table 52. MX-61h: Power Management Control 1

Name	Bits	Read/Write	Reset State	Description
En_i2s1	15	R/W	0'h	I2S1 Digital Interface Power Control 0'b: Power Down 1'b: Power On
En_i2s2	14	R/W	0'h	I2S2 Digital Interface Power Control 0'b: Power Down 1'b: Power On
reserved	13	R/W	0'h	Reserved
Pow_dac_l_1	12	R/W	0'h	Analog DACL1 Power Control 0'b: Power Down 1'b: Power On
Pow_dac_r_1	11	R/W	0'h	Analog DACR1 Power Control 0'b: Power Down 1'b: Power On
reserved	10:3	R	0'h	Reserved
Pow_adc_l	2	R/W	0'h	Analog ADCL Power Control 0'b: Power Down 1'b: Power On
Pow_adc_r	1	R/W	0'h	Analog ADCR Power Control 0'b: Power Down 1'b: Power On
Reserved	0	R	0'h	Reserved

8.37. MX-62h: Power Management Control 2

Default: 0000'h

Table 53. MX-62h: Power Management Control 2

Name	Bits	Read/Write	Reset State	Description
Pow_adc_stereo1_filter	15	R/W	0'h	Stereo1 ADC Digital Filter Power Control 0'b: Power Down 1'b: Power On
Pow_adc_stereo2_filter	14	R/W	0'h	Stereo2 ADC Digital Filter Power Control 0'b: Power Down 1'b: Power On
reserved	13:12	R	0'h	Reserved
Pow_dac_stereo1_filter	11	R/W	0'h	Stereo1 DAC Digital Filter Power Control 0'b: Power Down 1'b: Power On

Name	Bits	Read/Write	Reset State	Description
Pow_dac_stereo2_filter	10	R/W	0'h	Stereo2 DAC Digital Filter Power Control 0'b: Power Down 1'b: Power On
Pow_pdm	9	R/W	0'h	PDM Interface Power Control 0'b: Power down 1'b: Power on
Reserved	8:0	R	0'h	Reserved

8.38. MX-63h: Power Management Control 3

Default: 00C0'h

Table 54. MX-63h: Power Management Control 3

Name	Bits	Read/Write	Reset State	Description
Pow_vref1	15	R/W	0'h	VREF1 Power Control 0'b: Power Down 1'b: Power On
En_fastb1	14	R/W	0'h	VREF1 Fast Mode Control 0'b: Fast VREF 1'b: Slow VREF, (For good analog performance)
Pow_main_bias	13	R/W	0'h	MBIAS Power Control 0'b: Power Down 1'b: Power On
Pow_lout	12	R/W	0'h	LOUTMIX Power Control 0'b: Power Down 1'b: Power On
Pow_bg_bias	11	R/W	0'h	MBIAS Bandgap Power Control 0'b: Power Down 1'b: Power On
reserved	10:8	R	0'h	Reserved
En_l_hp	7	R/W	1'h	Left Headphone Amp Power Control 0'b: Power Down 1'b: Power On
En_r_hp	6	R/W	1'h	Right Headphone Amp Power Control 0'b: Power Down 1'b: Power On
En_amp_hp	5	R/W	0'h	Improve HP Amp Driving 0'b: Disable 1'b: Enable
Pow_vref2	4	R/W	0'h	VREF2 Power Control 0'b: Power Down 1'b: Power On
En_fastb2	3	R/W	0'h	VREF2 Fast Mode Control 0'b: Fast VREF 1'b: Slow VREF, (For good analog performance)
Reserved	2	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
Ldo_dvo	1:0	R/W	0’h	LDO Output Control 00’b: 1.1V 01’b: 1.2V 10’b: 1.3V 11’b: 1.4V

8.39. MX-64h: Power Management Control 4

Default: 0000’h

Table 55. MX-64h: Power Management Control 4

Name	Bits	Read/Write	Reset State	Description
Pow_bst1	15	R/W	0’h	MIC BST1 Power Control 0’b: Power Down 1’b: Power On
Pow_bst2	14	R/W	0’h	MIC BST2 Power Control 0’b: Power Down 1’b: Power On
Pow_bst3	13	R/W	0’h	MIC BST3 Power Control 0’b: Power Down 1’b: Power On
Reserved	12	R	0’h	Reserved
Pow_micbias1	11	R/W	0’h	MICBIAS1 Power Control 0’b: Power Down 1’b: Power On
reserved	10	R/W	0’h	reserved
Pow_pll	9	R/W	0’h	PLL Power Control 0’b: Power Down 1’b: Power On
reserved	8:6	R	0’h	Reserved
Pow_bst1_op2	5	R/W	0’h	MIC1 SE Mode Control 0’b: For differential mode 1’b: For single-end mode
Pow_bst2_op2	4	R/W	0’h	MIC2 SE Mode Control 0’b: For differential mode 1’b: For single-end mode or line-input mode
Pow_bst3_op2	3	R/W	0’h	MIC3 SE Mode Control 0’b: For differential mode 1’b: For single-end mode
Pow_jd_m	2	R/W	0’h	JD_Multilevel Power Control 0’b: Power down 1’b: Power on
Pow_jd2	1	R/W	0’h	JD2 Power Control 0’b: Power down 1’b: Power on
Pow_jd3	0	R/W	0’h	JD3 Power Control 0’b: Power down 1’b: Power on

8.40. MX-65h: Power Management Control 5

Default: 0000'h

Table 56. MX-65h: Power Management Control 5

Name	Bits	Read/Write	Reset State	Description
Pow_outmixl	15	R/W	0'h	OUTMIXL Power Control 0'b: Power Down 1'b: Power On
Pow_outmixr	14	R/W	0'h	OUTMIXR Power Control 0'b: Power Down 1'b: Power On
reserved	13:12	R	0'h	Reserved
Pow_recmixl	11	R/W	0'h	RECMIXL Power Control 0'b: Power Down 1'b: Power On
Pow_recmixr	10	R/W	0'h	RECMIXR Power Control 0'b: Power Down 1'b: Power On
reserved	9:0	R	0'h	Reserved

8.41. MX-66h: Power Management Control 6

Default: 0000'h

Table 57. MX-66h: Power Management Control 6

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0'h	Reserved
Pow_outvoll	13	R/W	0'h	OUTVOLL Power Control 0'b: Power Down 1'b: Power On
Pow_outvolr	12	R/W	0'h	OUTVOLR Power Control 0'b: Power Down 1'b: Power On
Pow_hpovoll	11	R/W	0'h	HPOVOLL Power Control 0'b: Power Down 1'b: Power On
Pow_hpovolr	10	R/W	0'h	HPOVOLR Power Control 0'b: Power Down 1'b: Power On
Pow_inlvol	9	R/W	0'h	INLVOL Power Control 0'b: Power Down 1'b: Power On

Name	Bits	Read/Write	Reset State	Description
Pow_inrvol	8	R/W	0’h	INRVOL Power Control 0’b: Power Down 1’b: Power On
reserved	7:0	R	0’h	Reserved

8.42. MX-6Ah: Private Register Index

Default: 0000’h

Table 58. MX-6Ah: Private Register Index

Name	Bits	Read/Write	Reset State	Description
reserved	15:8	R	0’h	reserved
Pr_index	7:0	R/W	0’h	PR Register Index

8.43. MX-6Ch: Private Register Data

Default: 0000’h

Table 59. MX-6Ch: Private Register Data

Name	Bits	Read/Write	Reset State	Description
Pr_data	15:0	R/W	0’h	PR Register Data

8.44. MX-70h: I2S1 Digital Interface Control

Default: 8000'h

Table 60. MX-70h: I2S1 Digital Interface Control

Name	Bits	Read/Write	Reset State	Description
Sel_i2s1_ms	15	R/W	1'h	I2S1 Digital Interface Mode Control 0'b: Master Mode 1'b: Slave Mode
Reserved	14:12	R	0'h	Reserved
en_i2s1_out_comp	11:10	R/W	0'h	I2S1 Output Data Compress (For ADCDAT1 Output) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
en_i2s1_in_comp	9:8	R/W	0'h	I2S1 Input Data Compress (For DACDAT1 Input) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
Inv_i2s1_bclk	7	R/W	0'h	I2S1 BCLK Polarity Control 0'b: Normal 1'b: Invert
reserved	6:4	R	0'h	Reserved
sel_i2s1_len	3:2	R/W	0'h	I2S1 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8 bits
sel_i2s1_format	1:0	R/W	0'h	I2S1 PCM Data Format Selection 00'b: I^2S format 01'b: Left justified 10'b: PCM Mode A (LRCK One Plus at Master Mode) 11'b: PCM Mode B (LRCK One Plus at Master Mode)

8.45. MX-71h: I2S2 Digital Interface Control

Default: 8000'h

Table 61. MX-71h: I2S2 Digital Interface Control

Name	Bits	Read/Write	Reset State	Description
Sel_i2s2_ms	15	R/W	1'h	I2S2 Digital Interface Mode Control 0'b: Master Mode 1'b: Slave Mode
reserved	14:12	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
en_i2s2_out_comp	11:10	R/W	0'h	I2S2 Output Data Compress (For ADCDAT2 Output) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
en_i2s2_in_comp	9:8	R/W	0'h	I2S2 Input Data Compress (For DACDAT2 Input) 00'b: OFF 01'b: μ law 10'b: A law 11'b: Reserved
inv_i2s2_bclk	7	R/W	0'h	I2S2 BCLK Polarity Control 0'b: Normal 1'b: Invert
reserved	6:4	R	0'h	Reserved
sel_i2s2_len	3:2	R/W	0'h	I2S2 Data Length Selection 00'b: 16 bits 01'b: 20 bits 10'b: 24 bits 11'b: 8bits
sel_i2s2_format	1:0	R/W	0'h	I2S2 PCM Data Format Selection 00'b: I^2S format 01'b: Left justified 10'b: PCM Mode A (LRCK One Plus at Master Mode) 11'b: PCM Mode B (LRCK One Plus at Master Mode)

8.46. MX-73h: ADC/DAC Clock Control 1

Default: 1104'h

Table 62. MX-73h: ADC/DAC Clock Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved
sel_i2s_pre_div1	14:12	R/W	1'h	I2S Clock Pre-Divider 1 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 3 011'b: ÷ 4 100'b: ÷ 6 101'b: ÷ 8 110'b: ÷ 12 111'b: ÷ 16
sel_i2s_bclk_ms2	11	R/W	0'h	I2S2 Master Mode Clock Relative of BCLK and LRCK 0'b: 16Bits (32FS) 1'b: 32Bits (64FS)

Name	Bits	Read/Write	Reset State	Description
sel_i2s_pre_div2	10:8	R/W	1'h	I2S Pre-Divider 2 000'b: ÷ 1 001'b: ÷ 2 010'b: ÷ 3 011'b: ÷ 4 100'b: ÷ 6 101'b: ÷ 8 110'b: ÷ 12 111'b: ÷ 16
reserved	7:4	R	0'h	Reserved
sel_dac_osr	3:2	R/W	1'h	Stereo DAC Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: 128Fs/3
sel_adc_osr	1:0	R/W	0'h	Stereo ADC Over Sample Rate Select 00'b: 128Fs 01'b: 64Fs 10'b: 32Fs 11'b: 128Fs/3

8.47. MX-74h: ADC/DAC Clock Control 2

Default: 0C00'h

Table 63. MX-74h: ADC/DAC Clock Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	0'h	Reserved
Dahpf_en	11	R/W	1'h	Stereo1/2 DAC Filter HPF Power Control 0'b: Disable 1'b: Enable
adhpf_en	10	R/W	1'h	Stereo1/2 ADC Filter HPF Power Control 0'b: Disable 1'b: Enable
reserved	9:0	R	0'h	Reserved

8.48. MX-75h: Digital Microphone Control

Default: 1400’h

Table 64. MX-75h: Digital Microphone Control

Name	Bits	Read/Write	Reset State	Description
en_dmic1	15	R/W	0’h	Enable DMIC1 Interface 0’b: Disable 1’b: Enable (Output DMIC clock)
Reserved	14	R	0’h	Reserved
sel_dmic1_l_edge	13	R/W	0’h	DMIC1 Left Channel Source Control 0’b: Latch from falling edge 1’b: Latch from rising edge
sel_dmic1_r_edge	12	R/W	1’h	DMIC1 Right Channel Source Control 0’b: Latch from falling edge 1’b: Latch from rising edge
Dmic1_data_pin_share	11:10	R/W	1’h	DMIC1 Data Pin Share Selection 00’b: ADCDAT2 01’b: IN1P 10’b: PDM_SCL 11’b: Reserved
reserved	9:8	R	0’h	Reserved
sel_dmic_clk	7:5	R/W	0’h	DMIC Clock Rate Control 000’b: 256*fs/2 001’b: 256*fs/3 010’b: 256*fs/4 011’b: 256*fs/6 100’b: 256*fs/8 101’b: 256*fs/12 Others: Reserved
reserved	4:0	R	0’h	Reserved

8.49. MX-77h: TDM Interface Control 1

Default: 0C00’h

Table 65. MX-77 TDM Interface Control 1

Name	Bits	Read / Write	Reset Status	Description
Intel_sel	15	R/W	0’h	I2S1 19.2MHz MCLK_In, Master Mode, 64FS/50FS Frame Rate Control 0’b: 64FS 1’b: 50FS
mode_sel	14	R/W	0’h	I2S / TDM Mode Control 0’b: Normal I2S Mode 1’b: TDM Mode
Tdmslot_sel	13:12	R/W	0’h	TDM Channel Number Select 00’b: 2ch 01’b: 4ch 10’b: 6ch 11’b: 8ch
channel_length	11:10	R/W	3’h	TDM Channel Length

				00’b: 16bit (For Slave Mode and Master Mode) 01’b: 20bit (For Slave Mode) 10’b: 24bit (For Slave Mode) 11’b: 32bit (For Slave Mode and Master Mode)
rx_adc_data_sel	9	R/W	0’h	ADC1/2 to ADCDAT Data Location 0’b: normal(adc1→slot0/1) If rx_adc_start=0’b =>Slot0/1/2/3 is ADC1_L/ADC1_R/ADC2_L/ADC2_R If rx_adc_start=1’b =>Slot4/5/6/7 is ADC1_L/ADC1_R/ADC2_L/ADC2_R 1’b: adc data swap(adc2→slot0/1) If rx_adc_start=0’b =>Slot0/1/2/3 is ADC2_L/ADC2_R/ADC1_L/ADC1_R If rx_adc_start=1’b =>Slot4/5/6/7 is ADC2_L/ADC2_R/ADC1_L/ADC1_R
rx_adc_start	8	R/W	0’h	ADC1/2 to ADCDAT Data Start Location 0’b: slot0 start 1’b: slot4 start
sel_i2s_rx_ch2	7:6	R/W	0’h	Data Swap for Slot0/1 in ADCDAT1 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R
sel_i2s_rx_ch4	5:4	R/W	0’h	Data Swap for Slot2/3 in ADCDAT1 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R
sel_i2s_rx_ch6	3:2	R/W	0’h	Data Swap for Slot4/5 in ADCDAT1 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R
sel_i2s_rx_ch8	1:0	R/W	0’h	Data Swap for Slot6/7 in ADCDAT1 00’b: L/R 01’b: R/L 10’b: L/L 11’b: R/R

8.50. MX-78h: TDM Interface Control 2

Default: 4000’h

Table 66. MX78 TDM control 2

Name	Bits	Read / Write	Reset Status	Description
sel_i2s_lrck_polarity	15	R/W	0’h	LRCK Polarity Inverter 0’b: Normal 1’b: Invert
tdm_ch_valid	14	R/W	1’h	TDM Slot Valid Data Control 0’b: CH0/1 Valid 1’b: CH0/1/2/3 Valid
tdm_ch_valid_en	13	R/W	0’h	TDM Slot Valid Data Enable Control

				0’b: Disable 1’b: Enable
Reserved	12	R	0’h	Reserved
lrck_pulse_sel	11	R/W	0’h	LRCK Pulse Width Select (Master Mode Only) 0’b: One BCLK width 1’b: One channel slot width
Reserved	10:8	R	0’h	Reserved
mute_tdm2_outl	7	R/W	0’h	ADC1 Left Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
mute_tdm2_outr	6	R/W	0’h	ADC1 Right Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
mute_tdm4_outl	5	R/W	0’h	ADC2 Left Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
mute_tdm4_outr	4	R/W	0’h	ADC2 Right Data Mute/Un-mute Control 0’b : Un-Mute 1’b : Mute
Reserved	3:0	R	0’h	Reserved

8.51. MX-79h: TDM Interface Control 3

Default: 0123’h

Table 67. MX79 TDM control 3

Name	Bits	Read / Write	Reset Status	Description
Reserved	15	R	0’h	Reserved
sel_i2s_tx_l_ch2	14:12	R/W	0’h	IF1_DAC1_L Data Selection 000’b: Slot0 001’b: Slot1 010’b: Slot2 011’b: Slot3 100’b: Slot4 101’b: Slot5 110’b: Slot6 111’b: Slot7
Reserved	11	R	0’h	Reserved
sel_i2s_tx_r_ch2	10:8	R/W	1’h	IF1_DAC1_R Data Selection 000’b: Slot0 001’b: Slot1 010’b: Slot2 011’b: Slot3 100’b: Slot4 101’b: Slot5 110’b: Slot6 111’b: Slot7
Reserved	7	R	0’h	Reserved
sel_i2s_tx_l_ch4	6:4	R/W	2’h	IF1_DAC2_L Data Selection 000’b: Slot0 001’b: Slot1 010’b: Slot2 011’b: Slot3 100’b: Slot4 101’b: Slot5 110’b: Slot6 111’b: Slot7
Reserved	3	R	0’h	Reserved
sel_i2s_tx_r_ch4	2:0	R/W	3’h	IF1_DAC2_R Data Selection 000’b: Slot0 001’b: Slot1 010’b: Slot2 011’b: Slot3 100’b: Slot4 101’b: Slot5 110’b: Slot6 111’b: Slot7

8.52. MX-80h: Global Clock Control

Default: 0000’h

Table 68. MX-80h: Global Clock Control

Name	Bits	Read/Write	Reset State	Description
sel_sysclk1	15:14	R/W	0’h	System Clock Source MUX Control 00’b: MCLK 01’b: PLL 10’b: Reserved 11’b: Reserved
sel_pll_sour	13:12	R/W	0’h	PLL Source Selection 00’b: From MCLK 01’b: From BCLK1 10’b: From BCLK2 11’b: Reserved
reserved	11:4	R	0’h	Reserved
sel_pll_pre_div	3	R/W	0’h	PLL Pre-Divider 0’b: ÷ 1 1’b: ÷ 2
reserved	2:0	R	0’h	Reserved

8.53. MX-81h: PLL Control 1

Default: 0000’h

Table 69. MX-81h: PLL Control 1

Name	Bits	Read/Write	Reset State	Description
Pll_n_code	15:7	R/W	0’h	PLL N[8:0] Code 000000000’b: Div 2 000000001’b: Div 3 … 111111111’b: Div 513
Reserved	6:5	R	0’h	Reserved
Pll_k_code	4:0	R/W	0’h	PLL K[4:0] Code 00000’b: Div 2 00001’b: Div 3 … 11111’b: Div 33

8.54. MX-82h: PLL Control 2

Default: 0000’h

Table 70. MX-82h: PLL Control 2

Name	Bits	Read/Write	Reset State	Description
Pll_m_code	15:12	R/W	0’h	PLL M[3:0] Code 0000’b: Div 2 0001’b: Div 3 … 1111’b: Div 17
Pll_m_bypass	11	R/W	0’h	Bypass PLL M Code 0’b : No bypass 1’b : Bypass
Reserved	10:0	R	0’h	Reserved

8.55. MX-83h: ASRC Control 1

Default: 0800’h

Table 71. MX-83h: ASRC Control 1

Name	Bits	Read/Write	Reset State	Description
sel_if1_asrc	15	R/W	0’h	Mode Select Control for I2S1 0’b : Normal Mode 1’b : ASRC Mode
reserved	14:13	R/W	0’h	Reserved
sel_if2_asrc	12	R/W	0’h	Mode Select Control for I2S2 0’b : Normal Mode 1’b : ASRC Mode
reserved	11:10	R/W	2’h	Reserved
sel_dmic1_mode	9	R/W	0’h	Select Control for ASRC Mode in DMIC1 Function 0’b : Normal Mode 1’b : ASRC Mode
reserved	8:0	R	0’h	Reserved

8.56. MX-84h: ASRC Control 2

Default: 0000’h

Table 72. MX-84h: ASRC Control 2

Name	Bits	Read/Write	Reset State	Description
en_if1_asrc	15	R/W	0’h	Enable Control for I2S1 0’b: Normal Mode 1’b: ASRC Mode
en_if2_asrc	14	R/W	0’h	Enable Control for I2S2 0’b: Normal Mode 1’b: ASRC Mode

Name	Bits	Read/Write	Reset State	Description
sel_stereo1_dac_mode	13	R/W	0'h	Select Control for Stereo1 DAC Filter 0'b: Normal Mode 1'b: ASRC Mode
sel_stereo2_dac_mode	12	R/W	0'h	Select Control for Stereo2 DAC Filter 0'b: Normal Mode 1'b: ASRC Mode
sel_adc_mode	11	R/W	0'h	Select Control for ADC Stereo Filter 0'b: Normal Mode 1'b: ASRC Mode
reserved	10:0	R/W	0'h	Reserved

8.57. MX-85h: ASRC Control 3

Default: 0008'h

Table 73. MX-85h: ASRC Control 3

Name	Bits	Read/Write	Reset State	Description
I2s1_asrcin_fsi_rate_manual	15:12	R/W	0'h	Set I2S1 Input Sample Rate 0'h: 48K 1'h: 96k 2'h: 192k 3'h: 32K 4'h: 48K 5'h: 96k 6'h: 192k 7'h: 32K 8'h: 48K 9'h: 96k A'h: 192k B'h: reserve C'h: 22.05K D'h: reserve E'h: 11.025K F'h: reserve
I2s2_asrcin_fsi_rate_manual	11:8	R/W	0'h	Set I2S2 Input Sample Rate 0'h: 48K 1'h: 96k 2'h: 192k 3'h: 32K 4'h: 48K 5'h: 96k 6'h: 192k 7'h: 32K 8'h: 48K 9'h: 96k A'h: 192k B'h: reserve C'h: 22.05K D'h: reserve E'h: 11.025K F'h: reserve
reserved	7:0	R/W	0'h	Reserved

8.58. MX-89h: ASRC Control 4

Default: 0000'h

Table 74. MX-89h: ASRC Control 4

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0'h	Reserved
i2s1_track_prediv	14:12	R/W	0'h	Set I2S1 Clock Division for Stereo Filter 000'b: div1 001'b: div2 010'b: div3 011'b: div4 100'b: div6 101'b: div8 110'b: div12 111'b: div16
reserved	11	R	0'h	Reserved
i2s2_track_prediv	10:8	R/W	0'h	Set I2S2 Clock Division for Mono Filter 000'b: div1 001'b: div2 010'b: div3 011'b: div4 100'b: div6 101'b: div8 110'b: div12 111'b: div16

Name	Bits	Read/Write	Reset State	Description
reserved	7:0	R/W	0'h	Reserved

8.59. MX-8Eh: HP Amp Control 1

Default: 0004'h

Table 75. MX-8Eh: HP Amp Control 1

Name	Bits	Read/Write	Reset State	Description
Smttrig_hp	15	R/W	0'h	Enable Softgen Trigger for Soft Mute Depop 0'b: Disable 1'b: Enable
reserved	14:10	R/W	0'h	Reserved
En_smt_l_hp	9	R/W	0'h	Enable HP_L Mute/Un-Mute Depop 0'b: Disbale 1'b: Enable
En_smt_r_hp	8	R/W	0'h	Enable HP_R Mute/Un-Mute Depop 0'b: Disbale 1'b: Enable
Pdn_hp	7	R/W	0'h	Capless Depop Power Down Control 0'b: Disbale 1'b: Enable
Softgen_rstn	6	R/W	0'h	Reset Softgen to Initialize SOFTP=1 0'b: Disbale 1'b: Reset
Softgen_rstp	5	R/W	0'h	Reset Softgen to Initialize SOFTP=0 0'b: Disbale 1'b: Reset
En_out_hp	4	R/W	0'h	Enable Headphone Output 0'b: Disable 1'b: Enable
Pow_pump_hp	3	R/W	0'h	Charge Pump Power Control 0'b: Power Down 1'b: Power On
En_softgen_hp	2	R/W	1'h	Power On Soft Generator 0'b: Power down 1'b: Power on
reserved	1	R/W	0'h	Reserved
Pow_capless	0	R/W	0'h	HP Amp All Power On Control 0'b: Power Down 1'b: Power On

8.60. MX-8Fh: HP Amp Control 2

Default: 1100’h

Table 76. MX-8Fh: HP Amp Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0’h	Reserved
Depop_mode_hp	13	R/W	0’h	Select HP Depop Mode 0’b: Depop mode 1 1’b: Depop mode 2
reserved	12:7	R/W	22’h	Reserved
En_depop_mode1	6	R/W	0’h	HP Depop Mode 1 Control 0’b: Disbale 1’b: Enable
reserved	5:0	R/W	0’h	Reserved

8.61. MX-93h: MICBIAS Control

Default: 2000’h

Table 77. MX-93h: MICBIAS Control

Name	Bits	Read/Write	Reset State	Description
Sel_micbias1	15	R/W	0’h	MICBIAS1 Output Voltage Control 0’b: 0.9 * MICVDD 1’b: 0.75 * MICVDD
reserved	14:12	R/W	2’h	Reserved
Pow_mic1_ovcd	11	R/W	0’h	MICBIAS1 Short Current Detector Control 0’b: Disable 1’b: Enable
Mic1_ovcd_th_sel	10:9	R/W	0’h	MICBIAS1 Short Current Detector Threshold 00’b: 600uA 01’b: 1500uA 1x’b: 2000uA Note: tolerance is 200uA
reserved	8:0	R/W	0’h	reserved

8.62. MX-94h: Jack Detection Control

Default: 0200’h

Table 78. MX-94h: Jack Detection Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:14	R	0’h	Reserved
Jad_cmp	13	R	0’h	JD2 Status

Name	Bits	Read/Write	Reset State	Description
Pullup_jd	11	R/W	0’h	JD2 Pull Up Control 0’b: Off 1’b: Pull up
Pulldown_jd	10	R/W	0’h	JD2 Pull Down Control 0’b: Off 1’b: Pull down
Reserved	9:7	R/W	4’h	Reserved
Jd_m_cmp	6:4	R	0’h	JD_M Output
Pullup_jd_m	3	R/W	0’h	JD_M Pull Up Control 0’b: Off 1’b: Pull up
Pulldown_jd_m	2	R/W	0’h	JD_M Pull Down Control 0’b: Off 1’b: Pull down
Reserved	1:0	R/W	0’h	Reserved

8.63. MX-B0h: EQ Control 1

Default: 2080’h

Table 79. MX-B0h: EQ Control 1

Name	Bits	Read/Write	Reset State	Description
eq_sour	15	R/W	0’h	EQ Path Control 0’b: DAC path 1’b: ADC path
eq_para_update	14	R/W	0’h	EQ Parameter Update Control 0’b: No action 1’b: Update parameter
reserved	13:7	R/W	41’h	Reserved
sta_hpf2	6	R	0’h	EQ High Pass Filter (HPF2) Status. 0’b: Normal 1’b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_hpf1	5	R	0’h	EQ High Pass Filter (HPF1) Status. 0’b: Normal 1’b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_bpf4	4	R	0’h	EQ Band-4 (BP4) Status. 0’b: Normal 1’b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

Name	Bits	Read/Write	Reset State	Description
sta_bpf3	3	R	0'h	EQ Band-3 (BP3) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_bpf2	2	R	0'h	EQ Band-2 (BP2) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_bpf1	1	R	0'h	EQ Band-1 (BP1) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.
sta_lpf	0	R	0'h	EQ Low Pass Filter (LPF) Status. 0'b: Normal 1'b: Overflow. This bit is set if overflow had ever occurred. Write 1 to clear it.

8.64. MX-B1h: EQ Control 2

Default: 0000'h

Table 80. MX-B1h: EQ Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:9	R	0'h	Reserved
reg_typ_hpf_en	8	R/W	0'h	EQ High Pass Filter1 Mode Control 0'b: High frequency shelving filter 1'b: 1st order Butterworth HPF (-20dB per decade)
reg_typ_lpf_en	7	R/W	0'h	EQ Low Pass Filter Mode Control 0'b: Low frequency shelving filter 1'b: 1st order Butterworth LPF (-20dB per decade)
en_hpf2	6	R/W	0'h	EQ High Pass 2nd Butterworth Filter (HPF) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
en_hpf1	5	R/W	0'h	EQ High Pass Filter (HPF) Control. 0'b: Disabled (bypass) and reset 1'b: Enabled
en_bpf4	4	R/W	0'h	EQ Band-4 (BP4) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.
en_bpf3	3	R/W	0'h	EQ Band-3 (BP3) shelving Filter Control. 0'b: Disabled and reset 1'b: Enabled.

Name	Bits	Read/Write	Reset State	Description
en_bpf2	2	R/W	0’h	EQ Band-2 (BP2) shelving Filter Control. 0’b: Disabled and reset 1’b: Enabled.
en_bpf1	1	R/W	0’h	EQ Band-1 (BP1) shelving Filter Control. 0’b: Disabled and reset 1’b: Enabled.
en_lpf	0	R/W	0’h	EQ Low Pass Filter (LPF) Filter Control. 0’b: Disabled and reset 1’b: Enabled.

8.65. MX-B4h: DRC/AGC Control 1

Default: 2206’h

Table 81. MX-B4h: DRC/AGC Control 1

Name	Bits	Read/Write	Reset State	Description
sel_drc_agc	15:14	R/W	0’h	DRC/AGC Enable 00’b: Disable DRC/AGC 01’b: Enable DRC to DAC Path 10’b: Disable DRC/AGC 11’b: Enable AGC to ADC Path
update_drc_agc_para m	13	R	1’h	Update DRC/AGC Parameter Write 1’b to update all DRC/AGC parameter
sel_drc_agc_atk	12:8	R/W	2’h	Select DRC/AGC attack rate (0.375dB/TU)❶ 00’h: 83 uSec 01’h: 0.167 mSec … 10’h: 5.46 Sec Others: Reserved
Drc_agc_rate_sel	7:5	R/W	0’h	DRC/AGC Rate Control for Sample Rate Change❸ 001’b: 48kHz 010’b: 96kHz 011’b: 192kHz 101’b: 44.1kHz 110’b: 88.2kHz 111’b: 176.4kHz Others: Reserved

Name	Bits	Read/Write	Reset State	Description
sel_rc_rate	4:0	R/W	6'h	Select DRC/AGC recovery rate (0.375dB/TU)❷ 00'h: 83 uSec 01'h: 0.167 mSec … 10'h: 5.46 Sec Others: Reserved

❶ attack time=(4*2^n)/Sample_Rate, n = MX-B4[12:8], default=0.33mS
❷ recovery time=(4*2^n)/Sample_Rate, n = MX-B4[4:0], default=5.3mS
❸ When change I2S's sample rate, the DRC/AGC rate control is need to be changed same with I2S's sample rate. When change the DRC/AGC rate, the parameter of DRC/AGC isn't need be modified.
When I2S's sample rate is below 48kHz, that need to set the DRC/AGC rate to 48kHz and re-calculate the DRC/AGC's parameter by I2S's sample rate.

8.66. MX-B5h: DRC/AGC Control 2

Default: 1F00'h

Table 82. MX-B5h: DRC/AGC Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0'h	Reserved
sel_drc_agc_post_bst	13:8	R/W	1f'h	DRC/AGC Digital Post-Boost Gain (0.375dB/step)❶ 00'h= -11.625dB …….. 3F'h= 12dB Others: Reserved
En_drc_agc_compress	7	R/W	0'h	DRC/AGC Compression Function Control 0'b: Disable 1'b: Enable
Sel_ratio	6:5	R/W	0'h	DRC/AGC Compression Ratio Selection 00'b: 1:1 01'b: 1:2 10'b: 1:4 11'b: 1:8

Name	Bits	Read/Write	Reset State	Description
sel_drc/agc_pre_bst	4:0	R/W	0'h	DRC/AGC Digital Pre-Boost Gain (1.5dB/step)❷ 00'h= 0dB 01'h= 1.5dB 02'h= 3dB 03'h= 4.5dB …….. 13'h= 28.5dBFS Others: Reserved

❶Gain table:

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	-11.625	16	10	-5.625	32	20	0.375	48	30	6.375	64	40	
1	1	-11.25	17	11	-5.25	33	21	0.75	49	31	6.75	65	41	
2	2	-10.875	18	12	-4.875	34	22	1.125	50	32	7.125	66	42	
3	3	-10.5	19	13	-4.5	35	23	1.5	51	33	7.5	67	43	
4	4	-10.125	20	14	-4.125	36	24	1.875	52	34	7.875	68	44	
5	5	-9.75	21	15	-3.75	37	25	2.25	53	35	8.25	69	45	
6	6	-9.375	22	16	-3.375	38	26	2.625	54	36	8.625	70	46	
7	7	-9	23	17	-3	39	27	3	55	37	9	71	47	
8	8	-8.625	24	18	-2.625	40	28	3.375	56	38	9.375	72	48	
9	9	-8.25	25	19	-2.25	41	29	3.75	57	39	9.75	73	49	
10	A	-7.875	26	1A	-1.875	42	2A	4.125	58	3A	10.125	74	4A	
11	B	-7.5	27	1B	-1.5	43	2B	4.5	59	3B	10.5	75	4B	
12	C	-7.125	28	1C	-1.125	44	2C	4.875	60	3C	10.875	76	4C	
13	D	-6.75	29	1D	-0.75	45	2D	5.25	61	3D	11.25			
14	E	-6.375	30	1E	-0.375	46	2E	5.625	62	3E	11.625			
15	F	-6	31	1F	0	47	2F	6	63	3F	12			

❷

DEC	HEX	Boost Gain	DEC	HEX	Boost Gain
0	0	0	16	10	24
1	1	1.5	17	11	25.5
2	2	3	18	12	27
3	3	4.5	19	13	28.5
4	4	6	20	14	
5	5	7.5	21	15	
6	6	9	22	16	
7	7	10.5	23	17	

8	8	12	24	18	
9	9	13.5	25	19	
10	A	15	26	1A	
11	B	16.5	27	1B	
12	C	18	28	1C	
13	D	19.5	29	1D	
14	E	21	30	1E	
15	F	22.5	31	1F	

8.67. MX-B6h: DRC/AGC Control 3

Default: 0000’h

Table 83. MX-B6h: DRC/AGC Control 3

Name	Bits	Read/Write	Reset State	Description
Noise_gate_boost	15:12	R/W	0’h	Select Compensation Gain When Signal is Below Noise Gate 0’h: 0dB 1’h: 3dB 2’h: 6dB … E’h: 42dB F’h: 45dB
sel_drc_agc_thmax	11:7	R/W	0’h	DRC/AGC Limiter Level (1.5dB/step) 00’h= 0dBFS 01’h= -1.5dBFS 02’h= -3dBFS 03’h= -4.5dBFS … 1F’h= -46.5dBFS
en_drc_agc_noise_gate	6	R/W	0’h	Enable Noise Gate function 0’b: Diaable 1’b: Enable
En_drc_agc_noise_gate_hold	5	R/W	0’h	Enable Noise Gate Hold Data Function 0’b: Disable 1’b: Enable

Name	Bits	Read/Write	Reset State	Description
sel_drc_agc_noise_th	4:0	R/W	0'h	Noise Gate Threshold (-1.5dB/step) 00'h: -36dBFS 01'h: -375dBFS …….. 1F'h: -82.5 dBFS

8.68. MX-BBh: Jack Detection Control 1

Default: 0000'h

Table 84. MX-BBh: Jack Detection Control 1

Name	Bits	Read/Write	Reset State	Description
sel_gpio_jd	15:13	R/W	0'h	Jack Detect Selection 000'b: OFF 001'b: GPIO1 010'b: GPIO2 011'b: GPIO3 100'b: GPIO4 101'b: GPIO5 110'b: GPIO6 Others: Reserved
reserved	12	R	0'h	Reserved
en_jd_hpo	11	R/W	0'h	Enable Jack Detect Trigger HPOUT 0'b: Disable 1'b: Enable
polarity_jd_tri_hpo	10	R/W	0'h	Select Jack Detect Polarity Trigger HPOUT 0'b: Low trigger 1'b: High trigger
en_jd_pdm_l	9	R/W	0'h	Enable Jack Detect Trigger PDM_L 0'b: Disable 1'b: Enable
polarity_jd_tri_pdm_l	8	R/W	0'h	Select Jack Detect Polarity Trigger PDM_L 0'b: Low trigger 1'b: High trigger
en_jd_pdm_r	7	R/W	0'h	Enable Jack Detect Trigger PDM_R 0'b: Disable 1'b: Enable
polarity_jd_tri_pdm_r	6	R/W	0'h	Select Jack Detect Polarity Trigger PDM_R 0'b: Low trigger 1'b: High trigger
reserved	5:4	R	0'h	Reserved
en_jd_lout	3	R/W	0'h	Enable Jack Detect Trigger LOUT 0'b: Disable 1'b: Enable

Name	Bits	Read/Write	Reset State	Description
polarity_jd_tri_lout	2	R/W	0'h	Select Jack Detect Polarity Trigger LOUT 0'b: Low trigger 1'b: High trigger
reserved	1:0	R/W	0'h	reserved

8.69. MX-BCh: Jack Detection Control 2

Default: 0000'h

Table 85. MX-BCh: Jack Detection Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:12	R	0'h	Reserved
Sel_jd_trigger	11:9	R/W	0'h	JD Trigger Source Selection 000'b: From sta_gpio_jd 001'b: From sta_jd1_1 010'b: From sta_jd1_2 011'b: From sta_jd2 Others: Reserved
reserved	8:0	R	0'h	Reserved

8.70. MX-BDh: IRQ Control 1

Default: 0000'h

Table 86. MX-BDh: IRQ Control 1

Name	Bits	Read/Write	Reset State	Description
en_irq_gpio_jd	15	R/W	0'h	IRQ Output Source Configure of GPIO Jack Detection Status 0'b: Disable 1'b: Enable
Reserved	14	R	0'h	Reserved
en_gpio_jd_sticky	13	R/W	0'h	Sticky Control for GPIO Jack Detect 0'b: Disable 1'b: Enable
Reserved	12	R	0'h	Reserved
inv_gpio_jd	11	R/W	0'h	GPIO Jack Detection Status Polarity 0'b: Normal 1'b: Output Invert
reserved	10	R	0'h	Reserved
en_irq_jd1_1	9	R/W	0'h	IRQ Output Source Configure of JD1_1 Jack Detection Status 0'b: Disable 1'b: Enable
en_jd1_1_sticky	8	R/W	0'h	Sticky Control for JD1_1 Jack Detect 0'b: Disable 1'b: Enable

Name	Bits	Read/Write	Reset State	Description
inv_jd1_1	7	R/W	0'h	JD1_1 Jack Detection Status Polarity 0'b: Normal 1'b: Output Invert
en_irq_jd1_2	6	R/W	0'h	IRQ Output Source Configure of JD1_2 Jack Detection Status 0'b: Disable 1'b: Enable
en_jd1_2_sticky	5	R/W	0'h	Sticky Control for JD1_2 Jack Detect 0'b: Disable 1'b: Enable
inv_jd1_2	4	R/W	0'h	JD1_2 Jack Detection Status Polarity 0'b: Normal 1'b: Output Invert
en_irq_jd2	3	R/W	0'h	IRQ Output Source Configure of JD2 Jack Detection Status 0'b: Disable 1'b: Enable
en_jd2_sticky	2	R/W	0'h	Sticky Control for JD2 Jack Detect 0'b: Disable 1'b: Enable
inv_jd2	1	R/W	0'h	JD2 Jack Detection Status Polarity 0'b: Normal 1'b: Output Invert
reserved	0	R	0'h	Reserved

8.71. MX-BEh: IRQ Control 2

Default: 0000'h

Table 87. MX-BEh: IRQ Control 2

Name	Bits	Read/Write	Reset State	Description
en_irq_micbias1_ovcd	15	R/W	0'h	IRQ Output Source Configure of MICBIAS1 Over Current Status 0'b: Disable 1'b: Enable
reserved	14:12	R/W	0'h	Reserved
en_micbias1_ovcd_sticky	11	R/W	0'h	Sticky Control for MICBIAS1 Over Current 0'b: Disable 1'b: Enable
reserved	10:8	R/W	0'h	Reserved
inv_micbias1_ovcd	7	R/W	0'h	MICBIAS1 over current status polarity 0'b: Normal 1'b: Output Invert
reserved	6:4	R	0'h	Reserved
Ovc_micbias1	3	R	0'h	MICBIAS1 Over Current Status Read: return status of each status pin Write: Write '0' to clear stick bit
Reserved	2:1	R	0'h	Reserved

Name	Bits	Read/Write	Reset State	Description
Sta_gpio8	0	R	0'h	GPIO8 Pin Status Read: return status of GPIO8 pin

8.72. MX-BFh: GPIO and Internal Status

Default: 0000'h

Table 88. MX-BFh: GPIO and Internal Status

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved
sta_jd2	14	R	0'h	JD2 Pin Status Read: return status of JD2 pin Write: Write '0' to clear stick bit
sta_jd1_2	13	R	0'h	JD1 Pin Status Read: return status of JD1_2 Write: Write '0' to clear stick bit
sta_jd1_1	12	R	0'h	JD1 Pin Status Read: return status of JD1_1 Write: Write '0' to clear stick bit
sta_gpio7	11	R	0'h	GPIO7 Pin Status Read: return status of GPIO7 pin
sta_gpio6	10	R	0'h	GPIO6 Pin Status Read: return status of GPIO6 pin
sta_gpio5	9	R	0'h	GPIO5 Pin Status Read: return status of GPIO5 pin
sta_gpio1	8	R	0'h	GPIO1 Pin Status Read: return status of GPIO1 pin
sta_gpio2	7	R	0'h	GPIO2 Pin Status Read: return status of each GPIO2 pin
sta_gpio3	6	R	0'h	GPIO3 Pin Status Read: return status of each GPIO3 pin
sta_gpio4	5	R	0'h	GPIO4 Pin Status Read: return status of each GPIO4 pin
sta_gpio_jd	4	R	0'h	GPIO_JD Status Read: Return status of Jack Detect Select output Write: Write '0' to clear stick bit
reserved	3:0	R	0'h	Reserved

8.73. MX-C0h: GPIO Control 1

Default: 0100’h

Table 89. MX-C0h: GPIO Control 1

Name	Bits	Read/Write	Reset State	Description
sel_gpio1_type	15	R/W	0’h	GPIO1 Pin Function Select 0’b: GPIO1 1’b: IRQ output
sel_gpio2_type	14	R/W	0’h	GPIO2 Pin Function Select 0’b: GPIO2 1’b: DMIC1_SCL
reserved	13:9	R	0’h	Reserved
Sel_i2s_pin	8	R/W	1’h	I2S-2 Pin Function Selection 0’b: I2S function pins 1’b: GPIO function pins
sel_gpio5_type	7	R/W	0’h	GPIO5 Pin Function Select 0’b: GPIO5 1’b: IRQ output
sel_gpio6_type	6	R/W	0’h	GPIO6 Pin Function Select 0’b: GPIO6 1’b: DMIC_SDA
sel_gpio7_type	5	R/W	0’h	GPIO7 Pin Function Select 0’b: GPIO7 1’b: IRQ output
sel_gpio8_type	4	R/W	0’h	GPIO8 Pin Function Select 0’b: GPIO8 1’b: DMIC_SDA
sel_gpio_pdm	3	R/W	0’h	GPIO7 & GPIO8 Pin Function Select 0’b: GPIO function 1’b: PDM function (GPIO7:PDM_SDA ; GPIO8: PDM_SCL)
Reserved	2:0	R	0’h	Reserved

8.74. MX-C1h: GPIO Control 2

Default: 0000’h

Table 90. MX-C1h: GPIO Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15	R	0’h	Reserved
sel_gpio5	14	R/W	0’h	GPIO5 Pin Configuration 0’b: Input 1’b: Output
sel_gpio5_logic	13	R/W	0’h	GPIO5 Output Pin Control 0’b: Drive Low 1’b: Drive High
inv_gpio5	12	R/W	0’h	GPIO5 Pin Polarity 0’b: Normal 1’b: Output Invert
sel_gpio4	11	R/W	0’h	GPIO4 Pin Configuration 0’b: Input 1’b: Output
sel_gpio4_logic	10	R/W	0’h	GPIO4 Output Pin Control 0’b: Drive Low 1’b: Drive High
inv_gpio4	9	R/W	0’h	GPIO4 Pin Polarity 0’b: Normal 1’b: Output Invert
sel_gpio3	8	R/W	0’h	GPIO3 Pin Configuration 0’b: Input 1’b: Output
sel_gpio3_logic	7	R/W	0’h	GPIO3 Output Pin Control 0’b: Drive Low 1’b: Drive High
inv_gpio3	6	R/W	0’h	GPIO3 Pin Polarity 0’b: Normal 1’b: Output Invert
sel_gpio2	5	R/W	0’h	GPIO2 Pin Configuration 0’b: Input 1’b: Output
sel_gpio2_logic	4	R/W	0’h	GPIO2 Output Pin Control 0’b: Drive Low 1’b: Drive High
inv_gpio2	3	R/W	0’h	GPIO2 Pin Polarity 0’b: Normal 1’b: Output Invert
sel_gpio1	2	R/W	0’h	GPIO1 Pin Configuration 0’b: Input 1’b: Output
sel_gpio1_logic	1	R/W	0’h	GPIO1 Output Pin Control 0’b: Drive Low 1’b: Drive High

Name	Bits	Read/Write	Reset State	Description
inv_gpio1	0	R/W	0'h	GPIO1 Pin Polarity 0'b: Normal 1'b: Output Invert

8.75. MX-C2h: GPIO Control 3

Default: 0000'h

Table 91. MX-C2h: GPIO Control 3

Name	Bits	Read/Write	Reset State	Description
reserved	15:9	R	0'h	Reserved
sel_gpio8	8	R/W	0'h	GPIO8 Pin Configuration 0'b: Input 1'b: Output
sel_gpio8_logic	7	R/W	0'h	GPIO8 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio8	6	R/W	0'h	GPIO8 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio7	5	R/W	0'h	GPIO7 Pin Configuration 0'b: Input 1'b: Output
sel_gpio7_logic	4	R/W	0'h	GPIO7 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio7	3	R/W	0'h	GPIO7 Pin Polarity 0'b: Normal 1'b: Output Invert
sel_gpio6	2	R/W	0'h	GPIO6 Pin Configuration 0'b: Input 1'b: Output
sel_gpio6_logic	1	R/W	0'h	GPIO6 Output Pin Control 0'b: Drive Low 1'b: Drive High
inv_gpio6	0	R/W	0'h	GPIO6 Pin Polarity 0'b: Normal 1'b: Output Invert

8.76. MX-CFh: SounzReal BassBack Control

Default: 0013’h

Table 92. MX-CFh: SounzReal BassBack Control

Name	Bits	Read/Write	Reset State	Description
En_bb	15	R/W	0’h	Enable BassBack Function 0’b: Disable 1’b: Enable
Sel_bb_coef	14:12	R/W	0’h	Select Control for BassBack Coefficient Type 000’b: Type A 001’b: Type B 010’b: Type C 011’b: Type D 1xx’b: Reserved
Reserved	11:6	R	0’h	Reserved
Bb_boost_gain	5:0	R/W	13’h	Select Control BassBack Boost Gain 000001’b: 1.5dB 000010’b: 3dB …… 010011’b: 24dB …… 011111’b: 42dB, with 1.5dB/Step

8.77. MX-D0h: SounzReal TruTreble Control 1

Default: 0680’h

Table 93. MX-D0h: SounzReal TruTreble Control 1

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R/W	0’h	Reserved
En_mp	13	R/W	0’h	Enable TruTreble Function 0’b: Disable 1’b: Enable
Mp_eg	12:8	R/W	6’h	TruTreble Enhanced Gain Control ❶ 00000’b: -11.625dB 00001’b: -10.5dB ……. 00110’b: -3dB ..... 10100’b: 7.5dB
reserved	7:0	R/W	80’h	Reserved

❶

Eg	Enhanced Gain	Eg	Enhanced Gain
1	-11.625dB	11	2.25 dB
2	-10.5 dB	12	3 dB
3	-9 dB	13	3.75 dB

4	-6.75 dB	14	4.5 dB
5	-4.5 dB	15	4.875 dB
6	-3 dB	16	5.625 dB
7	-1.875 dB	17	6 dB
8	-0.375 dB	18	6.375 dB
9	0.375 dB	19	7.125 dB
10	1.5 dB	20	7.5 dB

8.78. MX-D1h: SounzReal TruTreble Control 2

Default: 1C17’h

Table 94. MX-D1h: SounzReal TruTreble Control 2

Name	Bits	Read/Write	Reset State	Description
reserved	15:14	R	0’h	Reserved
mp_hp_wt	13	R/W	0’h	Select The Harmonic Weighting 0’b: a = 1/4(default) 1’b: a = 1/2
mp_og	12:8	R/W	1C’h	Select The Origin Signal Gain 00000’b: -5.8125dB 00001’b: -5.625dB … 10111’b: -0.5625 dB ... 11111’b: 12dB, with 0.1875dB/Step
reserved	7:6	R	0’h	Reserved
mp_hg	5:0	R/W	17’h	Select High Frequency Harmonic Gain (0.375 /step) 000000’b: -11.625dB 000001’b: -11.25dB … 010111’b: -3dB ... 111111’b: 12dB, with 0.375dB/Step

8.79. MX-D3h: Wind Filter Control 1

Default: B320’h

Table 95. MX-D3h: Wind Filter Control 1

Name	Bits	Read/Write	Reset State	Description
adj_hpf_2nd_en	15	R/W	1’h	Enable Adjustable 2nd Wind Filter 0'b : Disable (bypass mode) 1'b : Enable
adj_hpf_coef_l_sel	14:12	R/W	3’h	Left Channel Coefficient Sample Rate Selection 000'b: 8K/12K/16K Hz 001'b: 24K/32K Hz 010'b: 48K/44.1K Hz 011'b: 96K/88.2K Hz 100'b: 192K/176.4K Hz Others: Reserved
Reserved	11	R	0’h	Reserved
adj_hpf_coef_r_sel	10:8	R/W	2’h	Right Channel Coefficient Sample Rate Selection 000'b: 8K/12K/16K Hz 001'b: 24K/32K Hz 010'b: 48K/44.1K Hz 011'b: 96K/88.2K Hz 100'b: 192K/176.4K Hz Others: Reserved
reserved	7:0	R/W	20’h	Reserved

8.80. MX-D4h: Wind Filter Control 2

Default: 0000’h

Table 96. MX-D3h: Wind Filter Control 2

Name	Bits	Read/Write	Reset State	Description
Reserved	15:14	R	0’h	Reserved
adj_hpf_coef_l_num	13:8	R/W	0’h	Left Channel Coefficient Fine Parameter Selection (0 ~ 63)
Reserved	7:6	R	0’h	Reserved
adj_hpf_coef_r_num	5:0	R/W	0’h	Right Channel Coefficient Fine Parameter Selection (0 ~ 63)

8.81. MX-D9h: Soft Volume & ZCD Control

Default: 0809’h

Table 97. MX-D9h: Soft Volume & ZCD Control

Name	Bits	Read/Write	Reset State	Description
en_softvol	15	R/W	0’h	Digital Soft Volume Delay Control 0’b: Disable 1’b: Enable
Reserved	14	R	0’h	Reserved
en_o_svol	13	R/W	0’h	OUTVOLL/R Soft Volume Delay Control 0’b: Disable 1’b: Enable
en_hpo_svol	12	R/W	0’h	HPOVOLL/R Soft Volume Delay Control 0’b: Disable 1’b: Enable
en_zcd_digital	11	R/W	1’h	Digital Volume Zero Crossing Detection Control 0’b: Disable 1’b: Enable
pow_zcd	10	R/W	0’h	Power On Zero Crossing 0’b: Power Down 1’b: Power On
Reserved	9:8	R	0’h	Reserved
En_zcd_outmixr	7	R/W	0’h	OUTMIXR Mute/Un-Mute ZCD Control 0’b: Disable 1’b: Enable
En_zcd_outmixl	6	R/W	0’h	OUTMIXL Mute/Un-Mute ZCD Control 0’b: Disable 1’b: Enable
En_zcd_recmixr	5	R/W	0’h	RECMIXR Mute/Un-Mute ZCD Control 0’b: Disable 1’b: Enable
En_zcd_recmixl	4	R/W	0’h	RECMIXL Mute/Un-Mute ZCD Control 0’b: Disable 1’b: Enable
sel_svol	3:0	R/W	9’h	Soft Volume Change Delay Time 0000: 1 SVSYNC 0001: 2 SVSYNC 0010: 4 SVSYNC 0011: 8 SVSYNC 0100: 16 SVSYNC 0101: 32 SVSYNC 0110: 64 SVSYNC 0111: 128 SVSYNC 1000: 256 SVSYNC 1001: 512 SVSYNC 1010: 1024 SVSYNC Others: Reserved Note: SVSYNC=1/Fs, Step:-1.5dBFS

8.82. MX-FAh: General Control 1

Default: 0010’h

Table 98. MX-FAh: General Control 1

Name	Bits	Read/Write	Reset State	Description
Reserved	15:4	R	1’h	Reserved
En_detect_clk_sys	3	R/W	0’h	Enable MCLK Detection and Auto Switch to Internal Clock 0’b: Disable 1’b: Enable
Reserved	2:1	R/W	0’h	Reserved
Digital_gate_ctrl	0’h	R/W	0’h	MCLK Clock Gating Control 0’b: Gating input clock 0’b: Enable input clock

8.83. PR-3Dh: ADC/DAC RESET Control

Default: 2800’h

Table 99. PR-3Dh: ADC/DAC RESET Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R/W	1’h	Reserved
En_ckgen_adc	12	R/W	0’h	Enable ADC Clock Generator 0’b: Disable 1’b: Enable
Reserved	11	R/W	1’h	Reserved
Ckxen_dac	10	R/W	0’h	Enable DAC Clock1 Generator 0’b: Disable 1’b: Enable
En_ckgen_dac	9	R/W	0’h	Enable DAC Clock2 Generator 0’b: Disable 1’b: Enable
Reserved	8:0	R/W	0’h	Reserved

8.84. PR-63h: SounzReal OmniSound Control

Default: 3717’h

Table 100. PR-63h: SounzReal OmniSound Control

Name	Bits	Read/Write	Reset State	Description
spk3d_en	15	R/W	0’h	OmniSound Function Enable Control 0’b: Disable 1’b: Enable
spk3d_mix_mode	14:13	R/W	1’h	OmniSound L/R Channel Mixing Mode 00’b: L+R, 01’b: L+0.5R, 10’b: L+0.25R, 11’b: L+0.125R
spk3d_center_gain	12:8	R/W	17’h	OmniSound Center Part Gain Control 00’h: -23.25dB … 17’h: -6dB … 1f’h: 0dB, with 0.75dB/Step
Reserved	7:5	R/W	0’h	Reserved
spk3d_surr_gain	4:0	R/W	17’h	OmniSound Surround Part Gain Control 00’h: -17.25dB … 17’h: 0dB … 1f’h: 6dB, with 0.75dB/Step

8.85. PR-A0h: EQ Low Pass Filter Coefficient (LPF:a1)

Default: 1C10’h

Table 101. PR-A0h: EQ Low Pass Filter Coefficient (LPF:a1)

Name	Bits	Read/Write	Reset State	Description
lpf_a1	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.86. PR-A1h: EQ Low Pass Filter Gain (LPF:H0)

Default: 01F4’h

Table 102. PR-A1h: EQ Low Pass Filter Gain (LPF:H0)

Name	Bits	Read/Write	Reset State	Description
lpf_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.87. PR-A2h: EQ Band 1 Coefficient (BPF1:a1)

Default: C5E9’h

Table 103. PR-A2h: EQ Band 1 Coefficient (BPF1:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf1_a1	15:0	R/W	C5E9’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.88. PR-A3h: EQ Band 1 Coefficient (BPF1:a2)

Default: 1A98’h

Table 104. PR-A3h: EQ Band 1 Coefficient (BPF1:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf1_a2	15:0	R/W	1A98’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.89. PR-A4h: EQ Band 1 Gain (BPF1:H0)

Default: 1D2C’h

Table 105. PR-A4h: EQ Band 1 Gain (BPF1:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf1_h0	15:0	R/W	1D2C’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.90. PR-A5h: EQ Band 2 Coefficient (BPF2:a1)

Default: C882’h

Table 106. PR-A5h: EQ Band 2 Coefficient (BPF2:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf2_a1	15:0	R/W	C882’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.91. PR-A6h: EQ Band 2 Coefficient (BPF2:a2)

Default: 1C10’h

Table 107. PR-A6h: EQ Band 2 Coefficient (BPF2:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf2_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.92. PR-A7h: EQ Band 2 Gain (BPF2:H0)

Default: 01F4’h

Table 108. PR-A7h: EQ Band 2 Gain (BPF2:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf2_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.93. PR-A8h: EQ Band 3 Coefficient (BPF3:a1)

Default: E904'h

Table 109. PR-A8h: EQ Band 3 Coefficient (BPF3:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf3_a1	15:0	R/W	E904'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.94. PR-A9h: EQ Band 3 Coefficient (BPF3:a2)

Default: 1C10'h

Table 110. PR-A9h: EQ Band 3 Coefficient (BPF3:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf3_a2	15:0	R/W	1C10'h	2's complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.95. PR-AAh: EQ Band 3 Gain (BPF3:H0)

Default: 01F4'h

Table 111. PR-AAh: EQ Band 3 Gain (BPF3:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf3_h0	15:0	R/W	01F4'h	2's complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.96. PR-ABh: EQ Band 4 Coefficient (BPF4:a1)

Default: E904'h

Table 112. PR-ABh: EQ Band 4 Coefficient (BPF4:a1)

Name	Bits	Read/Write	Reset State	Description
Bpf4_a1	15:0	R/W	E904'h	2's complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.97. PR-ACh: EQ Band 4 Coefficient (BPF4:a2)

Default: 1C10’h

Table 113. PR-ACh: EQ Band 4 Coefficient (BPF4:a2)

Name	Bits	Read/Write	Reset State	Description
Bpf4_a2	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.98. PR-ADh: EQ Band 4 Gain (BPF4:H0)

Default: 01F4’h

Table 114. PR-ADh: EQ Band 4 Gain (BPF4:H0)

Name	Bits	Read/Write	Reset State	Description
Bpf4_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.99. PR-AEh: EQ High Pass Filter 1 Coefficient (HPF1:a1)

Default: 1C10’h

Table 115. PR-AEh: EQ High Pass Filter 1 Coefficient (HPF1:a1)

Name	Bits	Read/Write	Reset State	Description
Hpf1_a1	15:0	R/W	1C10’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.100. PR-AFh: EQ High Pass Filter 1 Gain (HPF1:H0)

Default: 01F4’h

Table 116. PR-AFh: EQ High Pass Filter 1 Gain (HPF1:H0)

Name	Bits	Read/Write	Reset State	Description
Hpf1_h0	15:0	R/W	01F4’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.101. PR-B0h: EQ High Pass Filter 2 Coefficient (HPF2:a1)

Default: 2000’h

Table 117. PR-B0h: EQ High Pass Filter 2 Coefficient (HPF2:a1)

Name	Bits	Read/Write	Reset State	Description
Hpf2_a1	15:0	R/W	2000’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a1 should be in -2 ~ 1.99)

8.102. PR-B1h: EQ High Pass Filter 2 Coefficient (HPF2:a2)

Default: 0000’h

Table 118. PR-B1h: EQ High Pass Filter 2 Coefficient (HPF2:a2)

Name	Bits	Read/Write	Reset State	Description
Hpf2_a2	15:0	R/W	0000’h	2’s complement in 3.13 format. (The range is from –4~3.99, the a2 should be in -2 ~ 1.99)

8.103. PR-B2h: EQ High Pass Filter 2 Gain (HPF2:H0)

Default: 2000’h

Table 119. PR-B2h: EQ High Pass Filter 2 Gain (HPF2:H0)

Name	Bits	Read/Write	Reset State	Description
Hpf2_h0	15:0	R/W	2000’h	2’s complement in 3.13 format. (The range is from –4~3.99, the H0 should be in -4 ~ 3.99)

8.104. PR-B3h: EQ Pre Volume Control

Default: 0800’h

Table 120. PR-B3h: EQ Pre Volume Control

Name	Bits	Read/Write	Reset State	Description
Eq_pre_vol	15:0	R/W	0800’h	2’s complement in 5.11 format. (Default is 0dB) (The range is from –16~15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB])

8.105. PR-B4h: EQ Post Volume Control

Default: 0800’h

Table 121. PR-B4h: EQ Post Volume Control

Name	Bits	Read/Write	Reset State	Description
Eq_post_vol	15:0	R/W	0800’h	2’s complement in 5.11 format. (Default is 0dB) (The range is from –16~15.99, pre-gain should be in 0 ~ 15.99 [+24dB ~ -66dB])

8.106. MX-FEh: Vendor ID

Default: 10EC’h

Table 122. MX-FEh: Vendor ID

Name	Bits	Read/Write	Reset State	Description
Vendor_id	15:0	R	10EC’h	Vendor ID

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 123. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO Buffer	DBVDD	-0.3	-	3.63	V
Digital Core	DCVDD	-0.3	-	1.98	V
Analog	AVDD	-0.3	-	1.98	V
Analog	DACREF	-0.3	-	1.98	V
Headphone	CPVDD	-0.3	-	1.98	V
Micbias	MICVDD	-0.3	-	3.63	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C

9.1.2. Recommended Operating Conditions

Table 124. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DBVDD	1.71	1.8	3.6	V
Digital Core	DCVDD	1.1	1.2	1.9	V
Analog	AVDD	1.71	1.8	1.9	V
Analog	DACREF	1.71	1.8	1.9	V
Headphone	CPVDD	1.71	1.8	1.9	V
Micbias	MICVDD	3.0	3.3	3.6	V

9.1.3. Static Characteristics

Table 125. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	DBVDD+0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.35DBVDD	V
High Level Input Voltage	V_{IH}	0.65DBVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DBVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DBVDD	V
Output Buffer High Drive Current	-	0.6	1.8	4.3	mA
Output Buffer Low Drive Current	-	0.7	2.1	4.8	mA
Input Buffer Pull-Up Resistor	-	55	110	270	KΩ
Input Buffer Pull-Down Resistor	-	63	130	300	KΩ

Note: DBVDD=1.8V, DCVDD=1.2V, $T_{ambient}$=40°C.

9.2. Analog Performance Characteristics

Table 126. Analog Performance Characteristics

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
Line Inputs (Single-ended)	-	0.6	-	Vrms
MIC Inputs (Single-ended)	-	0.6	-	Vrms
MIC Inputs (Differential)	-	1.2	-	Vrms
Full Scale Output Voltage				
Line Outputs (Single-ended)	-	1.0	-	Vrms
Line Outputs (Differential)	-	1.0	-	Vrms
Headphone Amplifiers Outputs (For 10KOhm Load)	-	1.0	-	Vrms
Headphone Amplifiers Outputs (For 16Ohm Load)		0.7		Vrms
S/N Ratio				
Stereo DAC Direct to HP_L/R with 32Ohm	-	100	102	dBA
	-			
Line_In to Stereo ADC with 0dB (Single-end)		94	95	dBA
MIC_In to Stereo ADC with 0dB (Differential or Single-end)		94	95	dBA
MIC_In to Stereo ADC with 20dB and MICBIAS (Differential or Single-end)		89		dBA
MIC_In to Stereo ADC with 40dB and MICBIAS (Differential or Single-end)		78		dBA
MIC_In to Stereo ADC with 50dB and MICBIAS (Differential or Single-end)		68		dBA
Total Harmonic Distortion + Noise				
DAC Direct to HP_L/R with 16Ohm				
Po = 20mW/CH		-81	-83	dB
DAC Direct to HP_L/R with 10KOhm				
-3dBFS		-86		dB
Line_In to Stereo ADC with 0dB (Single-end)		-83		dB
MIC_In to Stereo ADC with 0dB (Differential or Single-end)		-83		dB
MIC_In to Stereo ADC with 20dB and MICBIAS (Differential or Single-end)		-81		dB
MIC_In to Stereo ADC with 40dB and MICBIAS (Differential or Single-end)		-74		dB
MIC_In to Stereo ADC with 50dB and MICBIAS (Differential or Single-end)		-65		dB
Power Consumption (Slave I2S Mode, 24-bit, SR: 44.1KHz)				
P_power down (No Clock Input)		<50		uW
P_playback (Stereo DAC to HP_OUT with 16 Ohm Load, With Clock, play silence)		<= 5.5		mW
P_playback (Stereo DAC to HP_OUT with 16 Ohm Load, With Clock, Po=1mW/CH)		<= 13		mW
P_record (LINE_IN to Stereo ADC, With Clock)		< 9		mW

Parameter	Min	Typ	Max	Units
Power Down Current				
$I_{DD\_1.8V}$	-	-	10	µA
$I_{DDD\_3.3V}$	-	-	10	µA
MICBIAS1 Output Voltage				
Setting 1	-	0.9*MICVDD	-	V
Setting 2	-	0.75*MICVDD	-	V
MICBIAS1 Drive Current				
MICBIAS = 0.9*MICVDD	-	4	-	mA

Note: Standard test conditions:
$T_{ambient}$=25°C
DBVDD=1.8V
DCVDD=1.2V
AVDD=1.8V
MICVDD=3.3V
CPVDD=1.8V
1kHz input sine wave; PCM Sampling frequency=48kHz; Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation

9.3. Signal Timing

9.3.1. I²C Control Interface

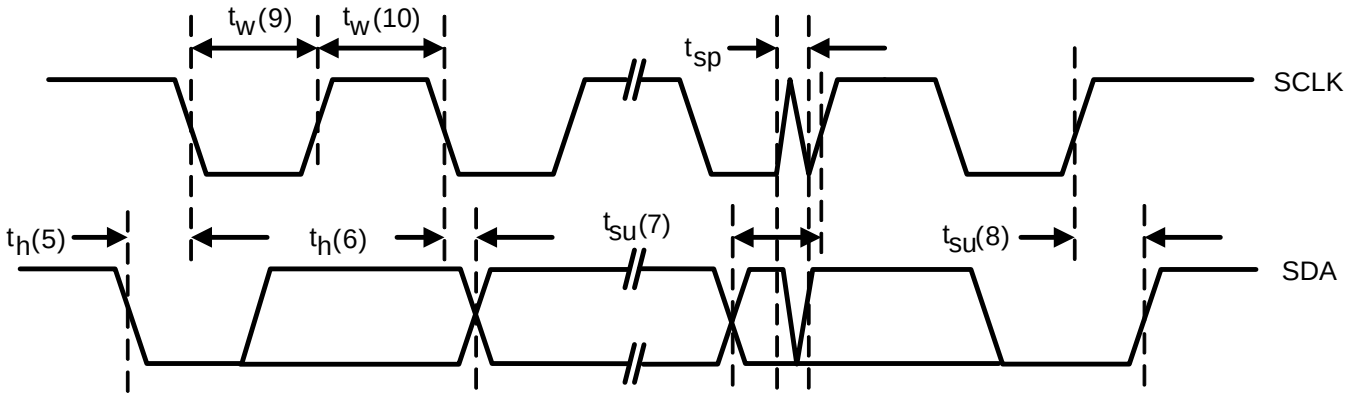


Figure 33. I²C Control Interface

Table 127. I²C Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Pulse Duration	$t_w(9)$	1.3	-	-	µs
Clock Pulse Duration	$t_w(10)$	600	-	-	ns
Clock Frequency	F	0	-	400K	Hz
Start Hold Time	$t_h(5)$	600	-	-	ns
Data Setup Time	$t_{su}(7)$	100	-	-	ns
Data Hold Time	$t_h(6)$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su}(8)$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

9.3.2. I²S/PCM Interface Master Mode

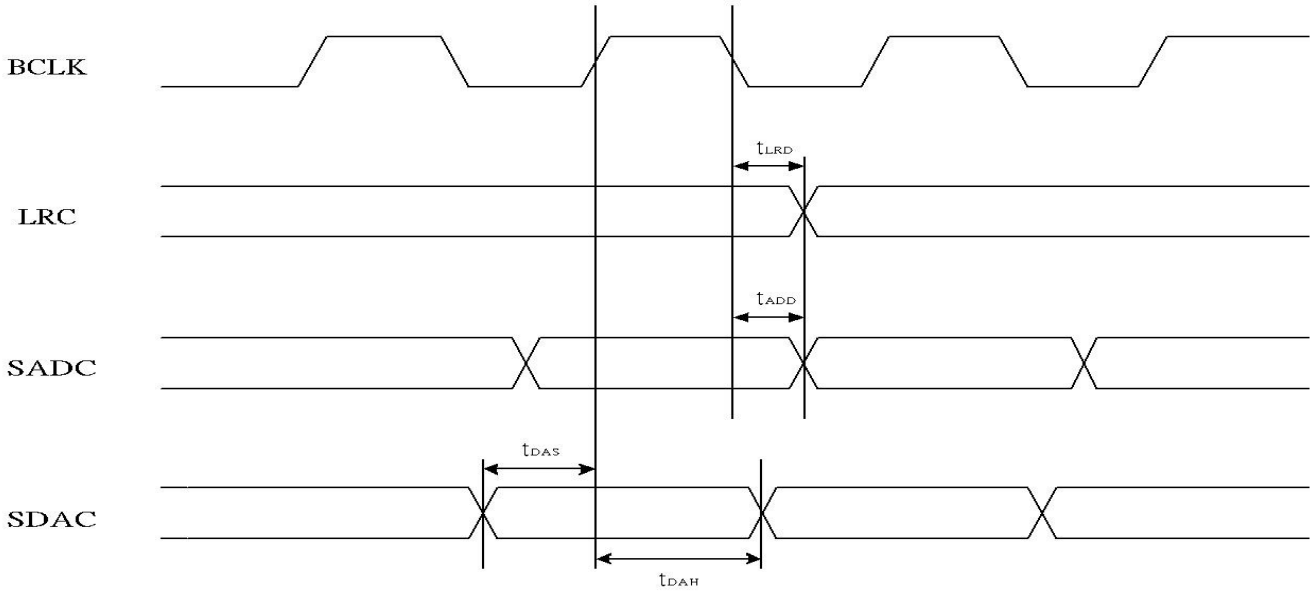


Figure 34. Timing of I²S/PCM Master Mode

Table 128. Timing of I²S/PCM Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

9.3.3. I²S/PCM Interface Slave Mode

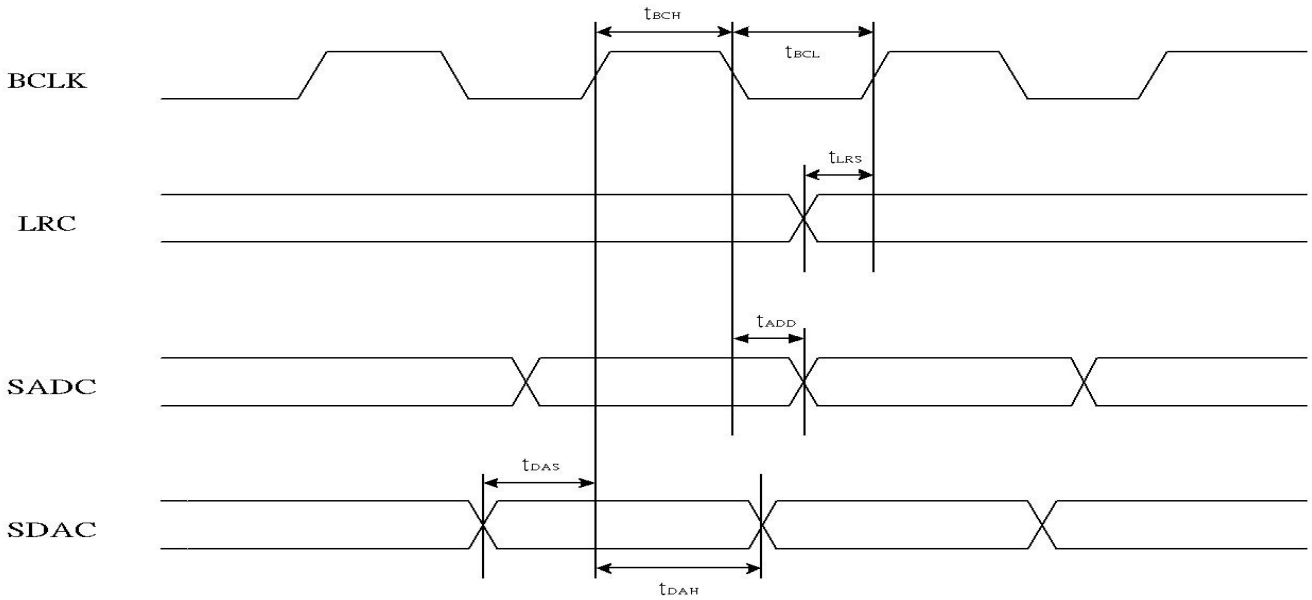
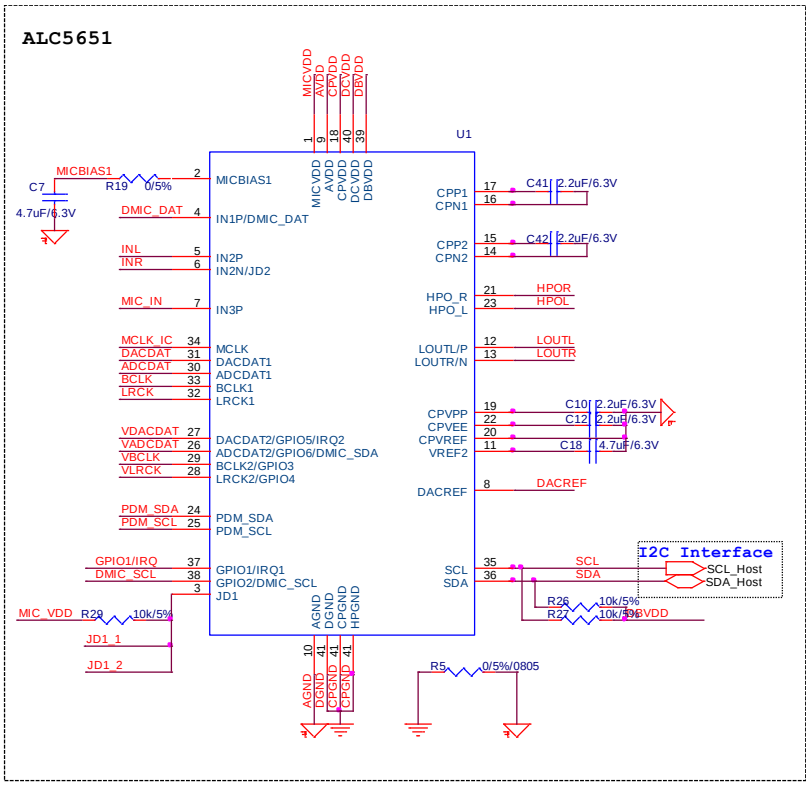


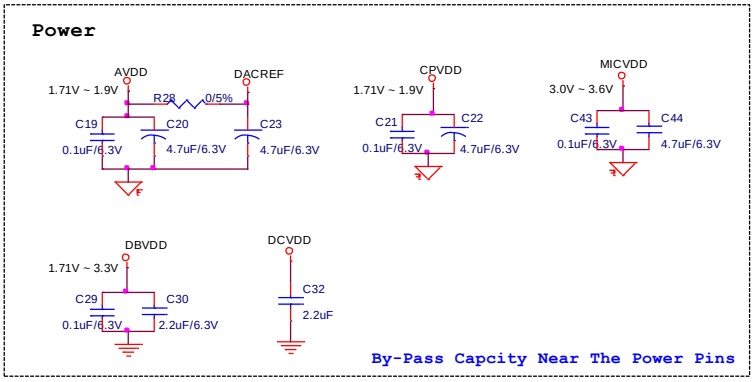
Figure 35. I²S/PCM Slave Mode Timing

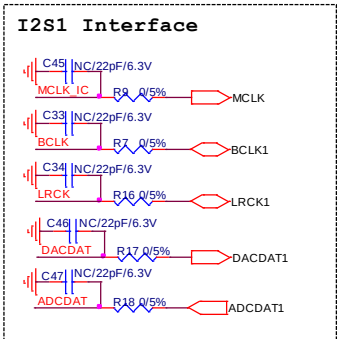
Table 129. I²S/PCM Slave Mode Timing

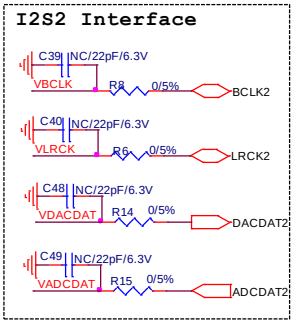
Parameter	Symbol	Min	Typ	Max	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

10. Application Circuits









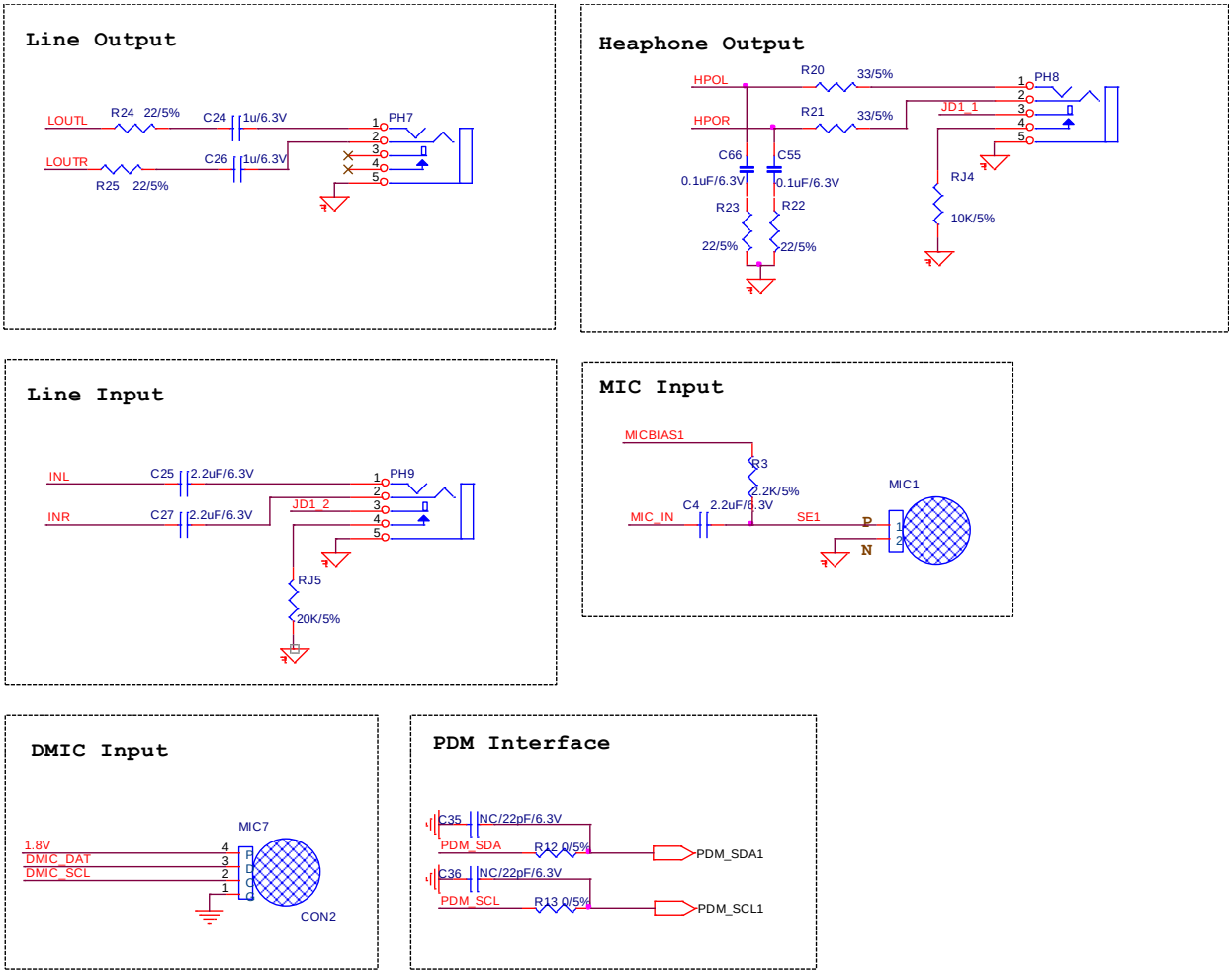
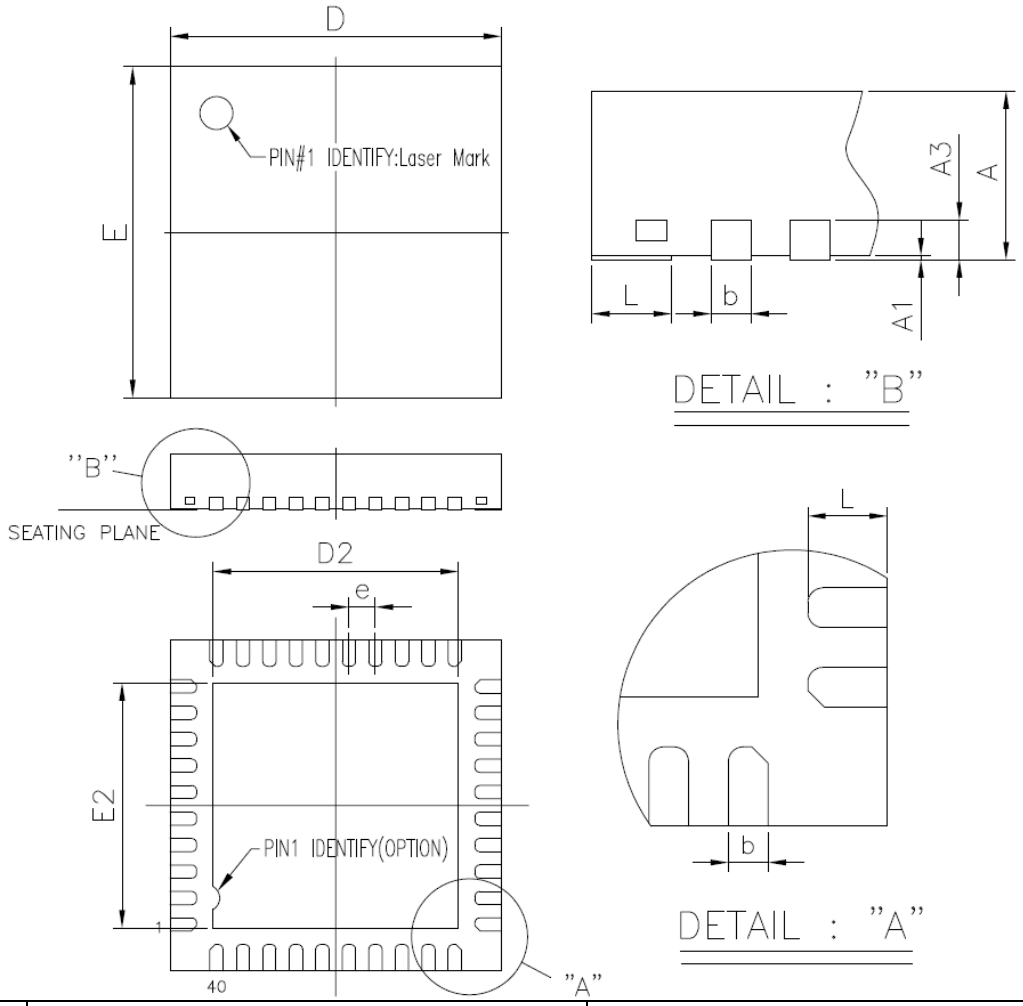


Figure 36. Application Circuit

11. Package Information

Plastic Quad Flat No-Lead Package 40 Leads 5x5mm^2 Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		5.00 BSC			0.197 BSC	
D2/E2	3.45	3.70	3.95	0.136	0.146	0.156
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes··

1. CONTROLLING DIMENSION·· MILLIMETER(mm).
2. REFERENCE DOCUMENTL·· JEDEC MO-220.

Figure 37. Package Dimension

12. Ordering Information

Table 130. Ordering Information

Part Number	Package	Status
ALC5651-CG	40-Pin QFN (5mm x 5mm) in 'Green' Package (Tray)	Mass Production
ALC5651-CGT	40-Pin QFN (5mm x 5mm) in 'Green' Package (Tape & Reel)	Mass Production
ALC5651R-CG	40-Pin QFN (5mm x 5mm) in 'Green' Package (Tray)	Mass Production
ALC5651R-CGT	40-Pin QFN (5mm x 5mm) in 'Green' Package (Tape & Reel)	Mass Production

* "R" is special for certain assign project purpose, not for general purpose.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047

www.realtek.com